Development of Flip Chip Assembly Services

MPW Services Center for IC / MEMS Prototyping

http://cmp.imag.fr

Grenoble - France
Motivation and objectives

Development of Flip Chip Assembly offer
- UBM and Solder bumping
- Substrates and micro assembly

Offer example
Motivation and objectives

Flip chip bonding advantages

• **Improving the IC performances:**
  - Reducing the parasites
  - Increasing the I/Os output speed & bandwidth
  - Improving the precision
  - Reducing the losses

• **Minimizing the assembly volume**
  - Miniaturization
  - Power Density
  - Optimized Commutation Cells

• **Increasing the thermal interfaces between the IC and the ambient**
  - Better thermal management
Flip chip prototyping flow

- **Major drawbacks**
  - Complex process flow
  - High engineering effort
  - Long processing delays
  - Increased cost
  - Increased failure risk

**Motivation and objectives**

Flip chip assembly services

**Design & fabrication**

- IC
- Substrate
- DRC OK?
- Fabrication
- Setup cost/NRE
- Scheduling process

**Flip chip assembly**

- UBM
- Bumping
- Scheduling process
- Setup cost/NRE
- Case study Flip Chip OK?

**CMP annual users meeting, 4 Feb. 2016, PARIS**
Objectives

- **Offer a wide range of Flip Chip Packaging options**
  - Bumping & mounting onto different substrates

- **Customer support:**
  - Add-on Flip Chip Packaging design kit (FCP Add-on on request)
  - Chip and substrate co-design verification

- **Turn around time optimization**
  - Single procedure avoiding case by case processing
  - Prequalified subcontractor engineering effort

- **Cost optimization:**
  - Setup and tooling cost sharing
UBM and Solder bumping

• Single die processing is possible!

- In order to reduce the setup cost and to minimize the engineering effort a fixed chip pad ring will be proposed (few options would be made available depending on the customers’ needs)
- Compatible with fine pitch substrates
- CMP Design verification
- Custom chip size and pad locations can be processed upon request
Substrates and micro assembly

• **Substrates:**
  - Pre-specified land patterning compatible with the fixed pad rings (few designs are possible depending on the customers’ needs)
  - Custom designs upon request
  - CMP Design verification
  - Minimized engineering effort (NRE)
  - Setup cost reduction
  - Substrate types: **organic, ceramic**

• **Micro assembly:**
  - CMP Chip/substrate co-design verification
  - Minimized engineering effort (NRE)
  - Setup cost reduction thanks to the normalized designs of the IC & the substrate
  - Substrate types: **organic, ceramic, silicon**
AMS circuits in 2015:

• Around 80% of the AMS circuits have:
  - Surface < 10mm²
  - I/Os < 84

• Around 80% of the packaged AMS circuits (65%) have:
  - Packages with < 84 I/Os
  - Square packages

ST circuits 28nm and 65nm in 2013 and 2014:

• Around 80% of the STM circuits have:
  - Surface < 1,6mm²
  - I/Os < 64

• All packaged STM circuits (80%) have:
  - Packages with < 64 I/Os
  - Square packages
Main challenges

• **Cost:**
  - Will I be charged for the total pad ring size if my IC is smaller? Yes, but CMP offer will be made so that it is cost effective even for the smallest IC sizes. However, each technology has a different cost gain. Worst case target is 20% reduction.

• **Size and I/O:**
  - My design is bigger and/or has more I/Os than the pad ring. Few options would be made possible depending on the customers’ needs.

**CMP Offer cost reduction for single die processing** as a function of the IC size for fixed pad ring:
*UBM + Bumping + Flip Chip assembly of 30 naked dies processed by PacTech*

**Example A:**
Pad ring 48 I/O S=8mm²

**Example B:**
Pad ring 100 I/O S=11,8mm²
Thank you!

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