2011

Design enablement and multi project wafer opportunity at LETI

Dr Carlo REITA, March 17th 2011

OUTLINE

■ **<u>FDSOI technology status</u>**
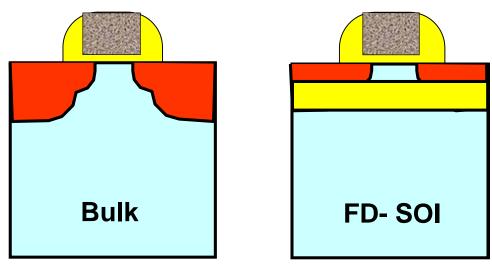
■ Circuit design platform status

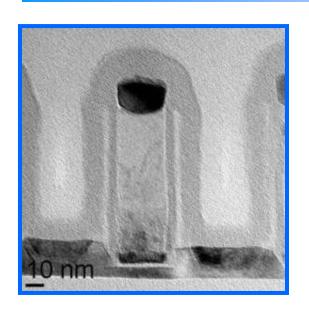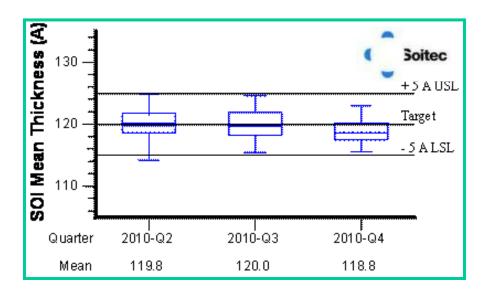■ LETI MPW offer

Introduction

Bulk **FD- SOI**

■ Use of SOI:

- Improve the scalability further than Bulk

- Reduce the variability thanks to undoped channel

- Limit the static power and dynamic power

  ➤ Low V_{DD} operation mandatory

FDSOI Technology

10 nm

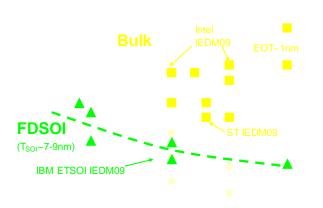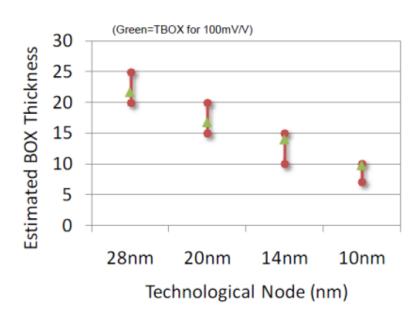| Quarter	2010-Q2	2010-Q3	2010-Q4
Mean	119.8	120.0	118.8

- Non-disruptive CMOS integration: planar device
- No channel doping, No Pocket implant
- Raised Source/Drain process
- Smart Substrate (UTBB) from SOITEC already within specification

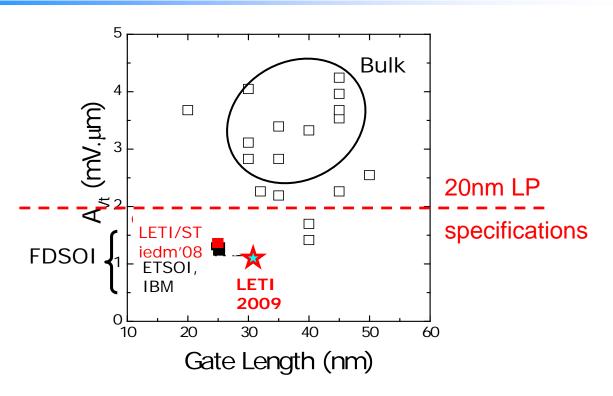# Electrostatic Performance

- **Enhanced electrostatic control compared to Bulk!**
- **Competitive with FinFET**
  - ↳ Good for Power control! (Pdyn ~V_{DD}^2)
- ↳ Can be maintained down to L_G=10nm with UTBOX

FDSOI results: Vt variability

- World record V_T mismatch !!
- Undoped SOI
  - today it already fully meets 20nm LP specification
  - largely exceed current nodes bulk results

Advantages of FDSOI for SoC
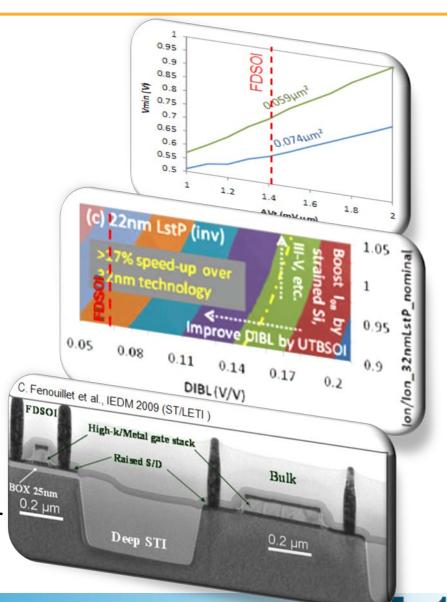
- **Excellent Electrostatic Control**
  - Ability to use undoped Si-channel → low variability → SRAM funtionnality at low Vcc
  - Low DIBL → increased speed performance

- **Using UTBOX**
  - Possibility of V_{th} control by Back-Bias (scalable)
  - Increased scalabililty below 16nm
  - Potential for Hybrid Bulk/FDSOI process for Power devices

C. Fenouillet et al., IEDM 2009 (ST/LETI)

courtesy of F.BOEUF, STM

STMicroelectronics

Leti

OUTLINE

■ FDSOI technology status

■ **<u>Circuit design platform status</u>**

■ LETI MPW offer

Circuit Design platform: **PDK for R&D**

- ■ **Technological library (Design & Layout)**
  - Devices MOS (Symbol, CDF)
  - Pcells MOS
  - Scribe 22 pads, contacts

  cadence®

- ■ **Electrical simulations (Eldo)**
  - Model cards,
  - Device sub circuits,
  - Corners setup

  Mentor Graphics®

- ■ **Physical verification and Layout finishing (Calibre)**
  - DRC verification file (Design Rules Checking),
  - LVS verification file (Layout Versus Schematic),
  - Dummies and Mask generation file

  Mentor Graphics®

- ■ **Parasitic extraction RC (Post-Layout, Star-RCXT)**
  - Process description file (itf → nxtgrd),
  - Mapping files (devices, layers),
  - Command file

  SYNOPSYS®

Circuit Design platform: **<u>PDK for R&D</u>**

■ Design platform deployment supported by the EUROSOI+ consortium (CA in European FP7 initiative)

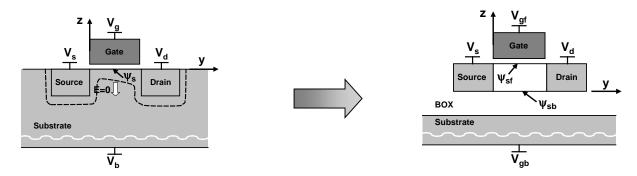■ Preliminary validation via bilateral collaborations

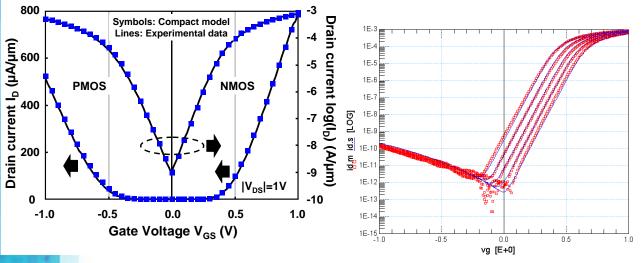# Circuit Design platform: FDSOI SPICE model

- **■** <u>LETI has developed</u> a surface potential compact model
  - today implemented as VerilogA plug-in
  - hard-coding in EDA tools possible
- **■** Analytical model which give access to all internal physical quantities:
  - Surface potentials at drain and source sides and at the punch-off
  - Saturation drain voltage
  - Terminals currents, GIDL, …
  - Charges
  - **SOI related physical effects** (Coupling, steeper subthreshold slope, Self-Heating)
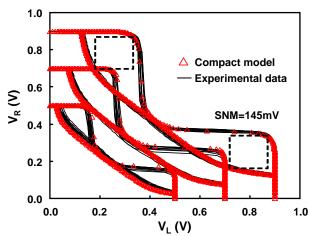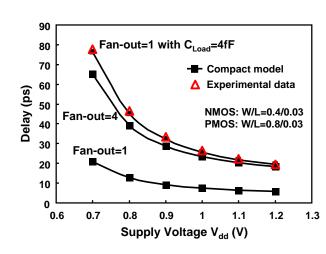
Circuit Design platform: Model calibration

- **Thick and thin BOX predictive 20nm model cards available**, calibrated on LETI FDSOI technology
- Used by STMicroelectronics for benchmarking (see F.Boeuf' presentation)
- Predictive model cards already developed down to 11nm node

OUTLINE

■ FDSOI technology status

■ Circuit design platform status

■ **LETI MPW offer**

MPW offer: content

- ■ **R&D oriented Design Kit made available via CMP service**
  - ● 20nm node FEOL with 65nm back-end in a first phase
  - ● 20nm node FEOL with 28nm back-end in a second phase
  - ● Evolution towards 16nm planned
- ■ **Specific acceptance rules**
  - ● no military or medical application circuits

CNRS-INPG-UJF

Offer outline

- ■ **R&D oriented Design Kit made available with initial parameter set**
  - ● min Lg=25nm
  - ● single Vt n- and p-MOSFETS with balanced Vth of ±0.4V
  - ● back end rules 65nm
  - ● 4 metal levels
  - ● ~40 cells library
  - ● place and route available

- ■ **Received designs implemented in one lot running at LETI**

MPW: timetable current run

- 11Q3 end – Distribution of DK via CMP
- 12Q2 (april) – GDS to be delivered to CMP
- 12Q3 beg. – Tape-out and run start
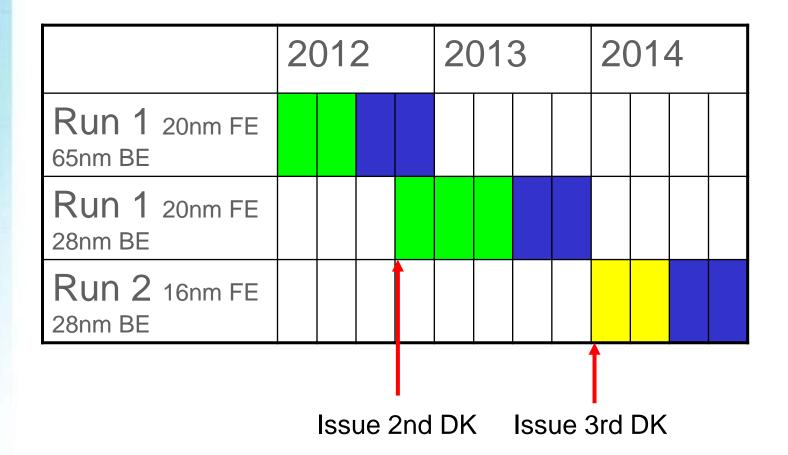- 13Q1 beginning – Silicon delivery

For more information on accessing the MPW go to CMP website: http://cmp.imag.fr/

For more information on the FDSOI offer contact: carlo.reita@cea.fr

MPW offer: current planning

	2012				2013				2014			
Run 1 20nm FE 65nm BE	🟩	🟩	🟦	🟦								
Run 1 20nm FE 28nm BE				🟩	🟩	🟩	🟦	🟦				
Run 2 16nm FE 28nm BE									🟨	🟨	🟦	🟦

Issue 2nd DK   Issue 3rd DK

Innovation for Industry

Loyalty
Entrepreneurship
Team work
Innovation

Loyalty
Entrepreneurship
Team work
Innovation

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