BCD8sP Technology Overview

Sense & Power and Automotive Technology R&D
Smart Power Technology

February 2015

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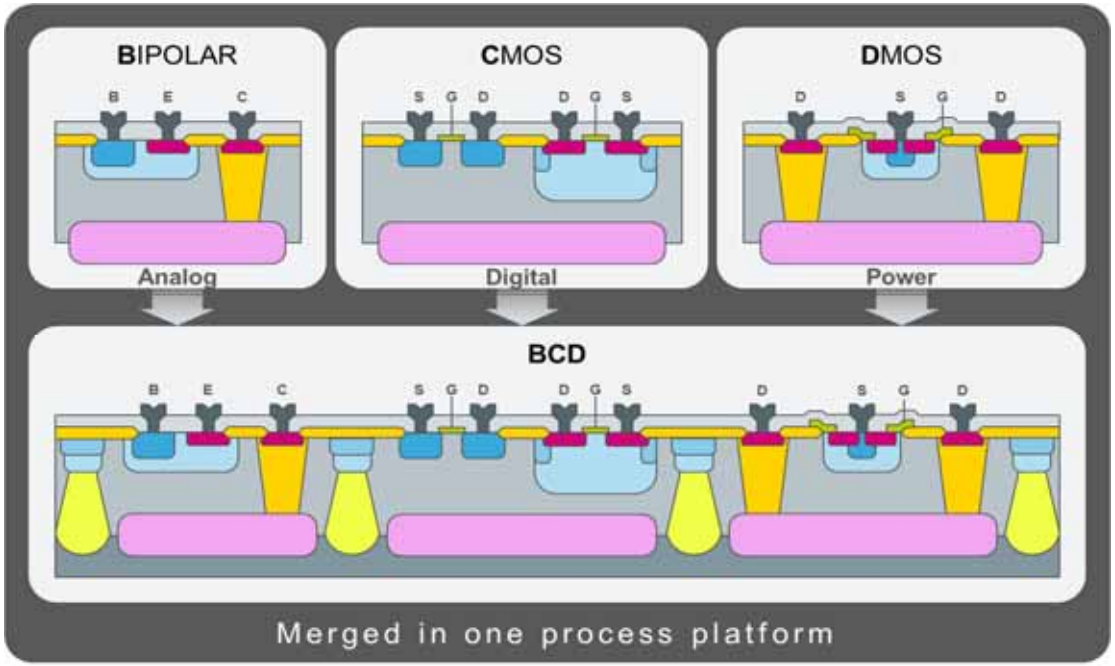
What is BCD ?

A concept invented by ST in the mid-80s [1][2][3] widely used today in the industry

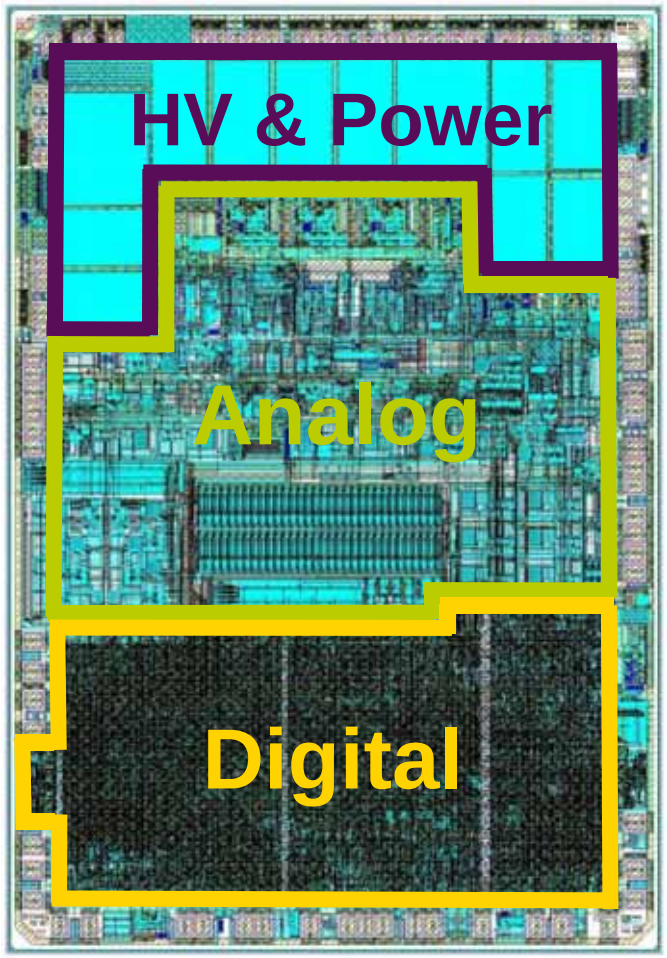


[1] ***Single Chip Carries Three technologies***, Electronics Week, December 10, **1984**

*[2] C. Cini, C. Contiero, C. Diazzi, P. Galbiati, D. Rossi, "**A New Bipolar, CMOS, DMOS Mixed Technology for Intelligent Power Applications"**,* ESSDERC '85 Proceedings, Aachen (Germany), September **1985**

*[3] A. Andreini, C. Contiero, P. Galbiati, "**A New Integrated Silicon Gate Technology Combining Bipolar Linear, CMOS Logic and DMOS Power Parts**",* IEEE Transactions on Electron Devices, Vol. ED-33 No.12, December **1986**

Analog + Digital + Power & HV on one chip



High Voltage or Power section (DMOS) to drive external loads

Analog blocks to interface the “external world” to the digital systems

Digital core (CMOS) for signal processing

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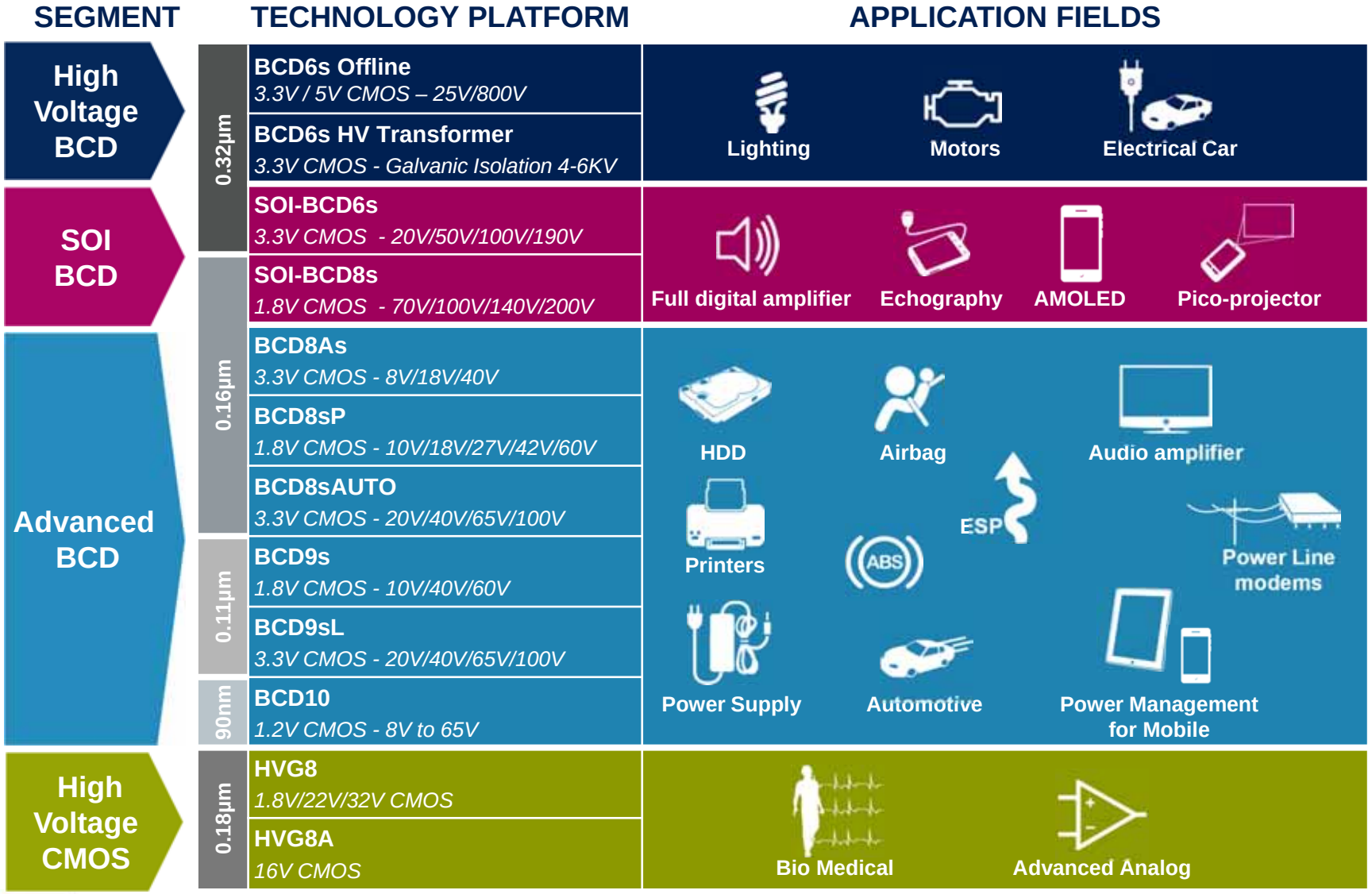
BCD Technology Segmentation



BCD Evolution in the “More than Moore” arena

Driven more by Process Customization
for Application Requirements
than by Reduction of Lithography Node

Trend towards Advanced Technology Nodes
compatible with availability of
Depreciated Advanced Manufacturing Plants

Long Lifetime
of Products and Process Generations

Always present demand for Cost Reduction

BCD in ST – Overview

- Solid know-how developed over three decades
  - Processes from 4.0 µm to 0.11 µm developed and produced

30 Years

- Unique voltage range offering
  - Large voltage range spanning multiple application fields

5 V to 800 V

- Advanced process nodes differentiated by application
  - Offers best in class HV devices with large CMOS integration capability

0.16 µm
0.11µm

- Process customization by application
  - Strong synergy between technology, design and application

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BCD8sP Overview

BCD8sP is a **0.16µm** Technology Platform dedicated to **Smart Power** applications with the following main features:

- Baseline 1.8V CMOS for **High Density Logic cores**
- **Best-in-class Power devices**: 10V - 18V - 27V - 42V
- Dual gate oxide process: 1.8V CMOS, 5V CMOS & Power Devices
- 4 Metal Levels with Thick Power metal
- Available memory: OTP, FTP (EEPROM)

Application examples:

- Hard Disk Drivers Power Combo
- Motor Drivers
- Printer
- DC-DC converter
- Power Management

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BCD8sP Device Portfolio

Low Voltage
- 1.8V CMOS
- 5V CMOS

High Voltage
- 10V/18V/27V/42V Power NMOS Isolated Drain
- 42V Power NMOS HS
- 15V/27V/32V/48V/60V nDrift MOS
- 15V/27V/32V/48V/60V pDrift MOS

Bipolars
- 5V NPN
- 5V PNP HP (Isolated Vertical)
- 18V PNP (Isolated Vertical)

Diodes
- 5V Zener, 5V Isolated Zener
- p+/Nwell, p+/HVnwell
- n+/Pwell, n+/Hvpwell

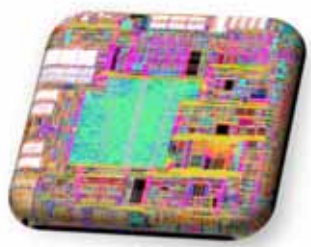
Capacitors
- 1.8V/5V poly capacitors
- 12V poly-poly capacitor
- MOM

Resistors
- Poly resistors (4 types), including HIPO resistor
- Diffused resistor

ESD & IPs
- 1.8V/5V/8V/18V/42V/60V ESD protection
- OTP & NVM libraries

BCD8sP Main Features

- 1.8V CMOS with HD Digital Library (90 kGates/mm^2)
- 5V CMOS and wide passive components offer for Analog design
- 4 Metal level BEOL with following options for Top Metal:
  - 3µm Thick Aluminum
  - 10µm Thick Copper (Re-Distribution Layer)



- **Best-in-class** Power devices with specification matching real application needs

Nch MOS POWER SPEC (full T range: -40 ° C ÷ 125 ° C)		POWER PERFORMANCE (T = 25 ° C)	
Max Operating Voltage (MOV)	Absolute Max Rating (AMR)	BVdss (TYP)	R_{ON} x A (mΩ x mm^2)
10 V	**12 V**	**14 V**	**2.9**
18 V	**25 V**	**29 V**	**8.7**
27 V	**32 V**	**36 V**	**14.2**
42 V	**46 V**	**57 V**	**28**

- Typical product masks count (based on option): **28 to 33**

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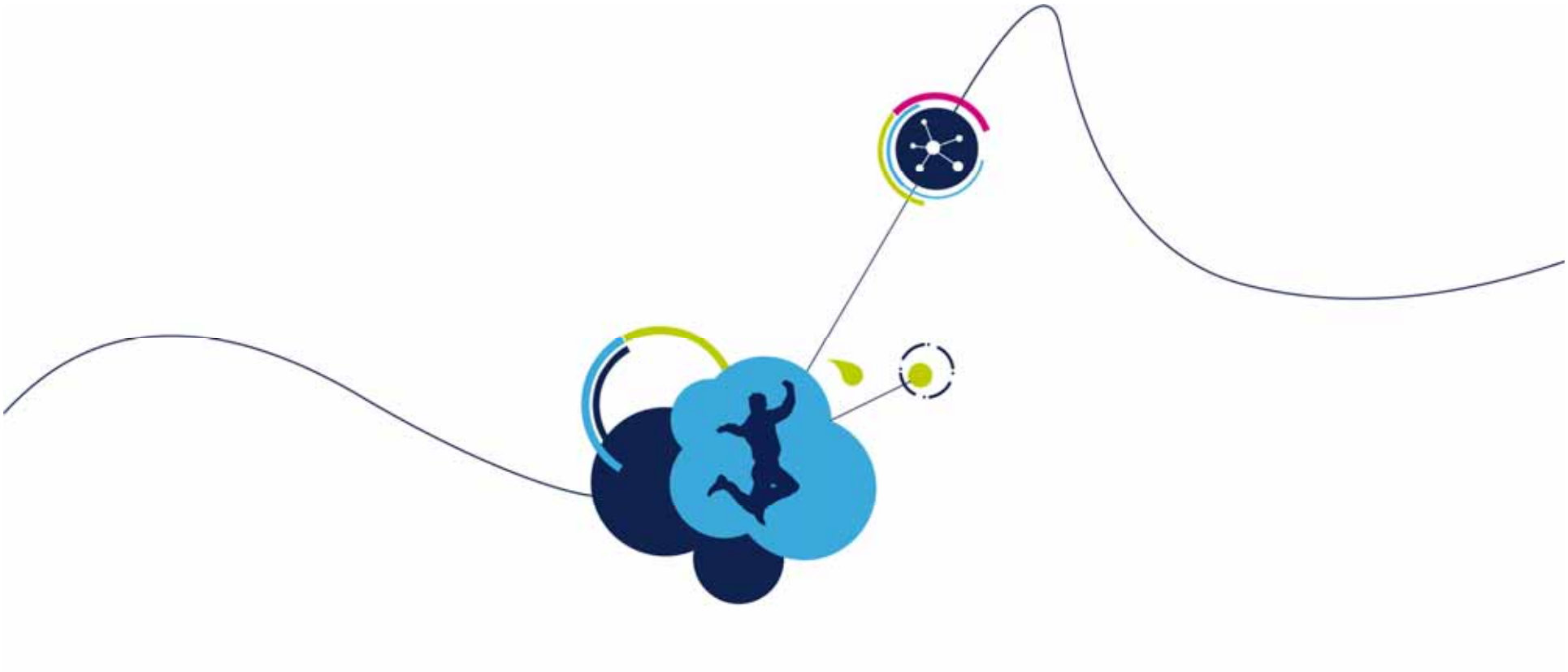

Design Platform: Design Kit, supported tools & Libraries

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Design Platform – Basic Tools Supported in PDK

Front-end/Schematic capture	EDA tools	EDA Vendors	Tool version (or newest)
Schematic Capture (Composer)	IC	Cadence	IC6.1.6.500.3
Design environment	ArtistKit	ST	5.9
	Spectre	Cadence	12.11.164
	Eldo	Mentor	13.1

Layout Entry & Finishing	EDA tools	EDA Vendors	Tool version (or newest)
Layout Placement	Virtuoso Layout Editor	Cadence	IC6.1.6.500.3
Layout Verification	Calibre ViPVS	Mentor Cadence	2013.1_14.11 13.10.286
Parasitic Extraction: interconnect RC	Star-RCXT	Synopsys	i-2013.12-1

Metal options available: 4M Al – 4M Cu RDL

Design Platform – Full List of supported Tools

Cadence

IC 6.1.6.500.3 (Virtuoso Framework)
Spectre 12.11.164 (Analog Simulator)
ViPVS 13.10.286 (Layout Verification)
mmsim 12.11.164 (Analog simulator environment)
incisiv 13.10.001 (Simulation Verification Environment)
Conformal 12.10.300 (Formal Verification)
Rc 12.20.000 (Synthesis)
edi 13.2usr3 (P&R)
IC 6.1.6.500.3 (VSR AnalogRouter)

Synopsys

Star-RCXT i-2013.12-1 (Parasitic Extraction
hsimplus i-2013.12 (Tx Level Simulator)
mvtools g-2012.09-4 (Static checker)
vcsmx h-2013.06-sp1 (Digitla simulator)
xa i-2013.12 (Tx Level Simulator)
Primetime h-2013.06-sp2 (STA)
PrimeRail f2011.12 (Digital IRDrop)
Synthesis h-2013.03-sp3
Tetramax h-2013.03-sp3 (ATPG)
Formality h-2013.03-sp3 (Formal Check)
Galaxy-ca h-2013.06-sp2 (Constraint Analyzer)
Iccompiler g-2012.06-sp5 (P&R)
Hercules y-2006.12-sp2-6 (Cheker for Prme Rail)

Mentor

Eldo/Eldo Premier 13.1 (transistor level)
Questa-ADMS 13.1 (mixed-signal cosimulation)
Calibre 2013.1_14.11 (Layout Verification)
QuestaSim 10.2.b (digital simulation)

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Design Platform – Digital Libraries/IPs

Digital Library	• BCD8000HDS – (1.8V CMOS)
SP Analog IPs	Macrocells_ESD • Dedicated library for HV protection
Memory Compilers	• Single port RAM (2 compilers) • OTP (1 to 16) x (8/16) bits • Cut service available on request
IO's Libraries	• 3V3FT 4MAI (3V capable 5V tolerant GPIO) • 5V0 4MAI (5V capable GPIO)
Power Devices Library	• «Ready-to-use» Power Devices layout • Cut service available on request

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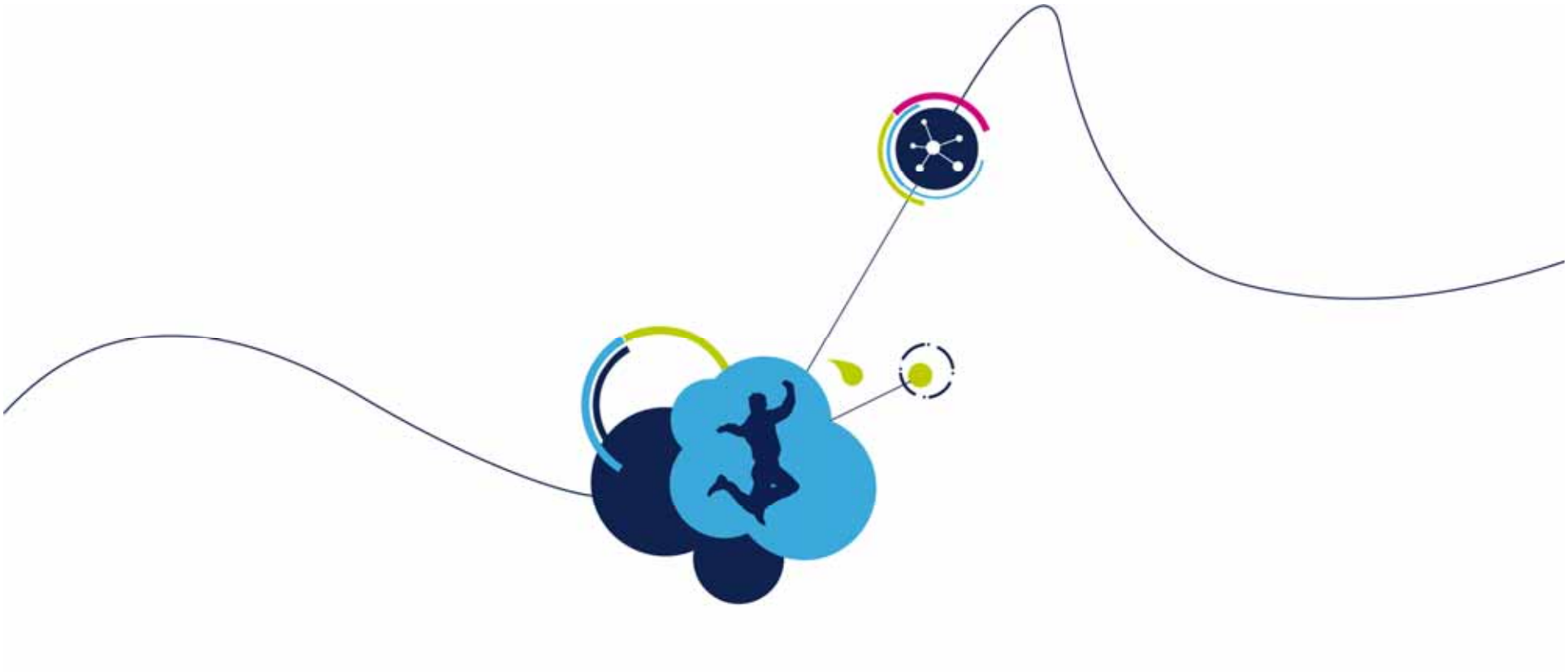

Schedule

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BCD8sP Design Timeline

• PDK / Design Platform availability	NOW
• Next MPW run	June 2015
• Last MPW in 2015	November 2015

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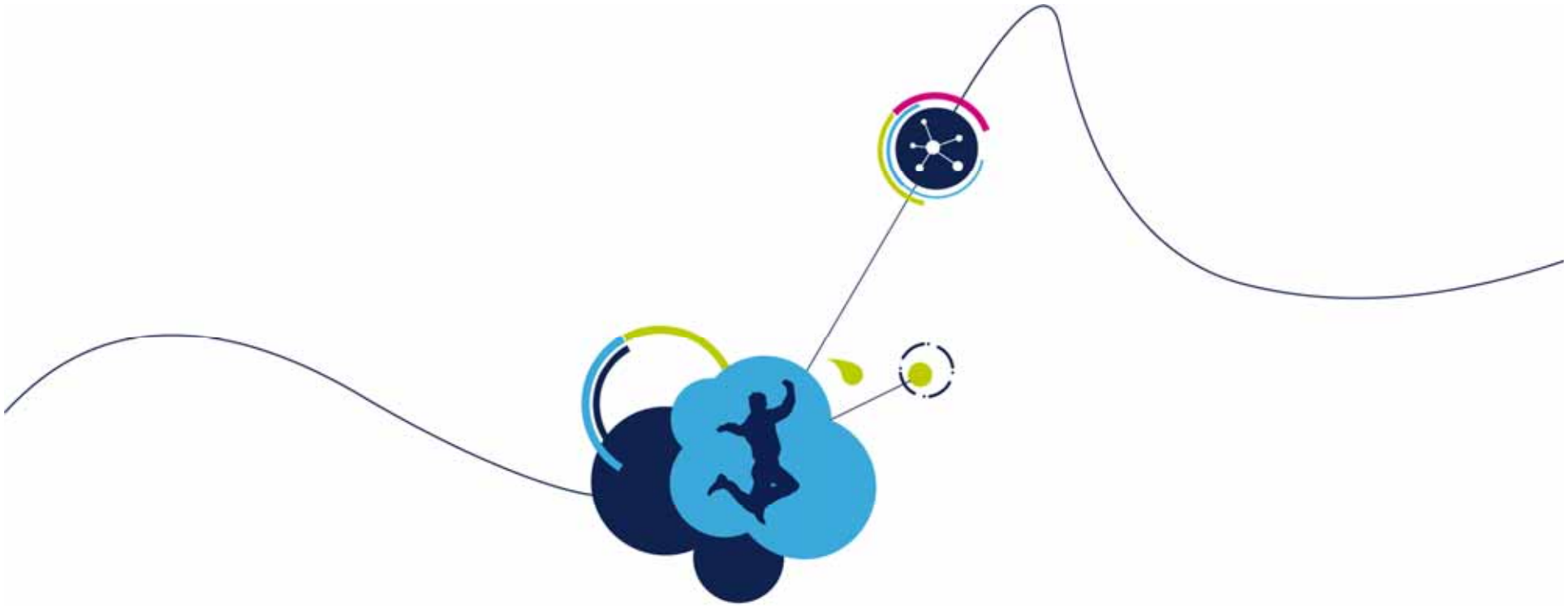

Thank You

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