Circuits Multi-Projets

Technology Processes & Runs in 2016

MPW Services Center for IC / MEMS Prototyping

http://cmp.imag.fr

Grenoble - France

web

Annual meeting agenda

09:20- Introduction, *Jean- Christophe Crébier, CMP*

09:30- Statistics and evolution for 2016, *Kholdoun Torki, CMP*

09:45- STMicroelectronics MPW services, *Romain Verly, CMP*

10:05- 28nm FD-SOI RTL to GDS design flow tutorial, new developments, *Christelle Rabache, CMP*

10:20- OxRAM memories: a disruptive technology for disruptive designs, *Luca Perniola, CEA LETI*

10:40 Break + Discussion

11:10- ams MPW services, *Kholdoun Torki, CMP*

11:30- Hot Topics at ams in 2017, *Andreas Wild, ams*

11:50- Flip-chip & Advanced packaging, *Lyubomir Kerachev & Olivier Guiller, CMP*

12:25- More than Moore MPW services, *Azedine Manaa, CMP*

12:40- Photonic IC design using PhoeniX Software solutions, *Luis Jorge, PhoeniX Software*

13:10 Lunch + Discussion

14:00- End of CMP users' annual meeting

Available Processes

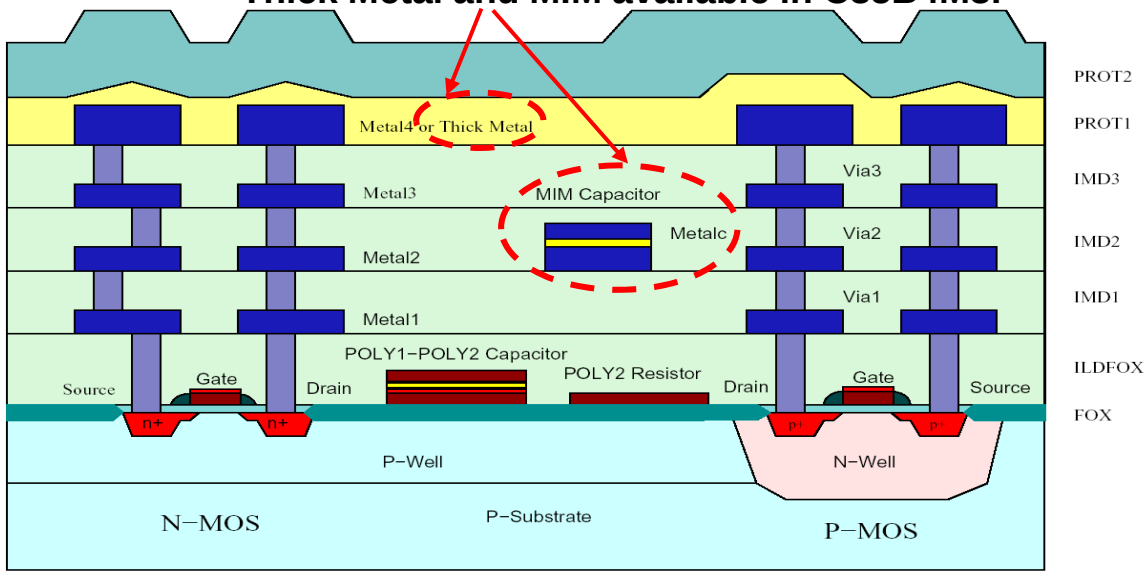
Process Name	Process Feature
C18A6	0.18µ CMOS
H18A6	0.18µ HV-CMOS
C35B4C2	0.35µ CMOS 3.3V
C35B4C3	0.35µ CMOS 3.3V / 5.0V
C35B4O1	0.35µ CMOS-Opto ARC
C35B4OA	0.35µ CMOS-Opto BARC New
S35D4M5	0.35µ SiGe BiCMOS
C35B4M3	0.35µ CMOS-RF
H35B4D3	0.35µ HV-CMOS
BYE / BYQ	0.8µ BiCMOS (available on request)

amu Process (0.35µ CMOS)

CMOS 0.35µ C35 (C35B4C3)

- 2 Layers Polysilicon, 4 Layers Metal, 3.3V / 5.0V, High Resistive Poly.
- 3.3V / 5.0V I/O pads.
- Peripheral cells with high driving capability (from 1mA to 24mA)
- Application : Analog, Digital, Mixed A/D, RF.
- Density : 18 kgates/mm^2
- Gate Delay: 100ps (NAND2 typical)
- Libraries : Digital and Analog Standard Cells + Pads + P-Cells.
- CORELIB qualified for 1.8V / 2.2V / 2.7V / 3.3V
- CORELIB_V5 qualified for 2.0V / 3.0V / 4.0V / 5.0V

Thick Metal and MIM available in C35B4M3.

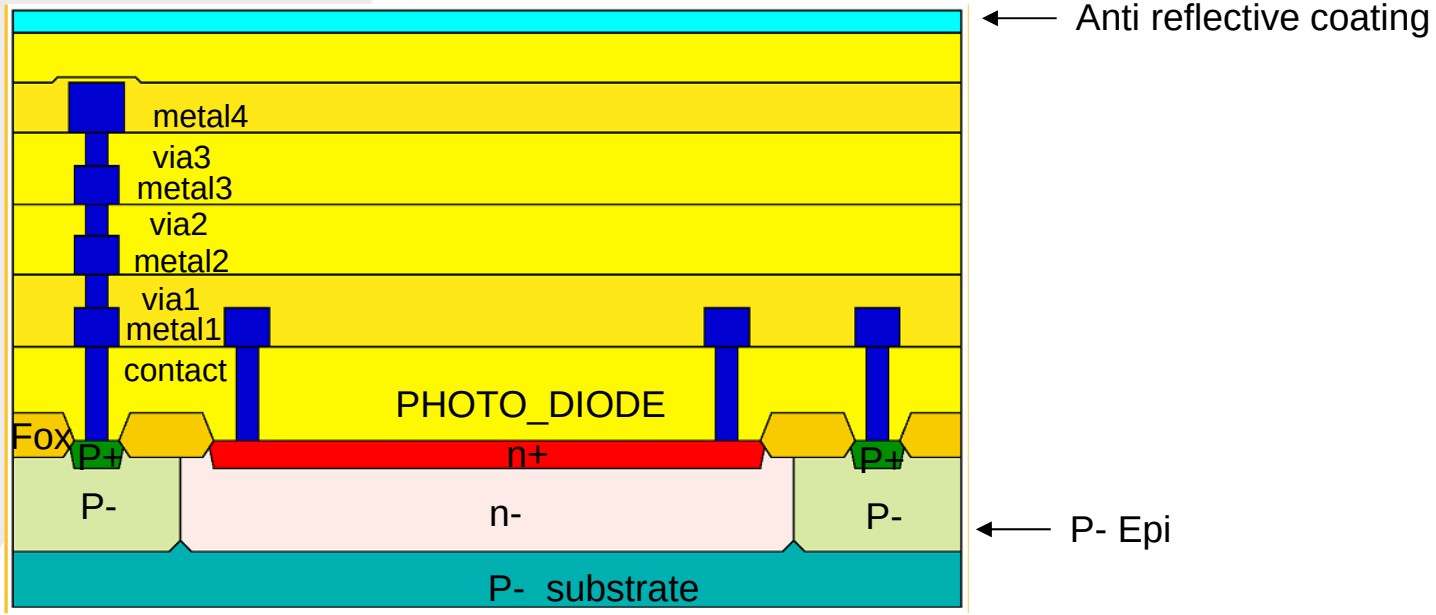


- **6 MPW runs scheduled in 2017.**
- **MPW Price : 650 Euro/mm^2**

CMOS-Opto 0.35µ

CMOS-Opto 0.35µ (C35B4O1)

- Planarization and anti-reflective coating allows better optical features.
- P-Epi wafers for lowering current leakage in the diode (lower dark current).



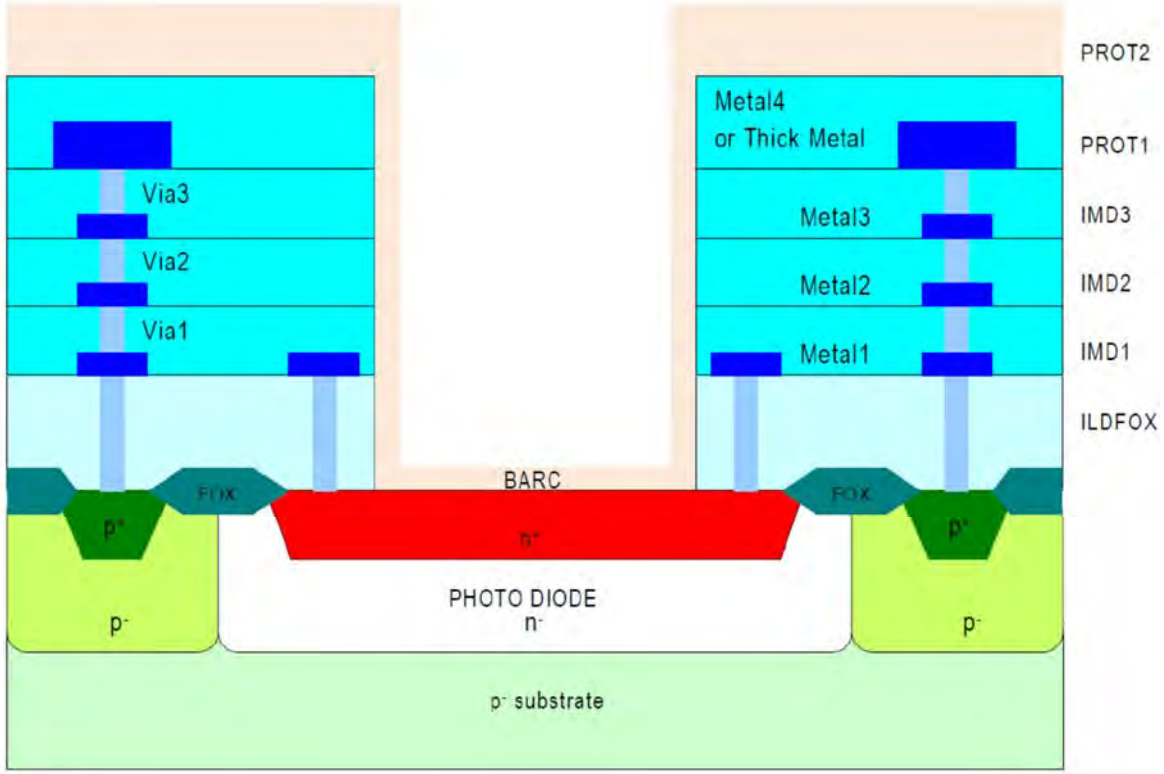
- Design-kit compatible with the 4 layers metal process option C35B4.
- Every C35 MPW run planned by CMP includes the CMOS-Opto option.

- **6 MPW runs scheduled in 2017.**
- **MPW New Price : 700 Euro/mm²**

CMOS-Opto BARC – C35B4OA

CMOS-Opto 0.35µ with Bottom Anti-Reflective Coating (BARC) (C35B4OA)

- Bottom Anti-Reflective Coating allows better sensitivity than ARC.
- P-Epi wafers for lowering current leakage in the diode (lower dark current).



New

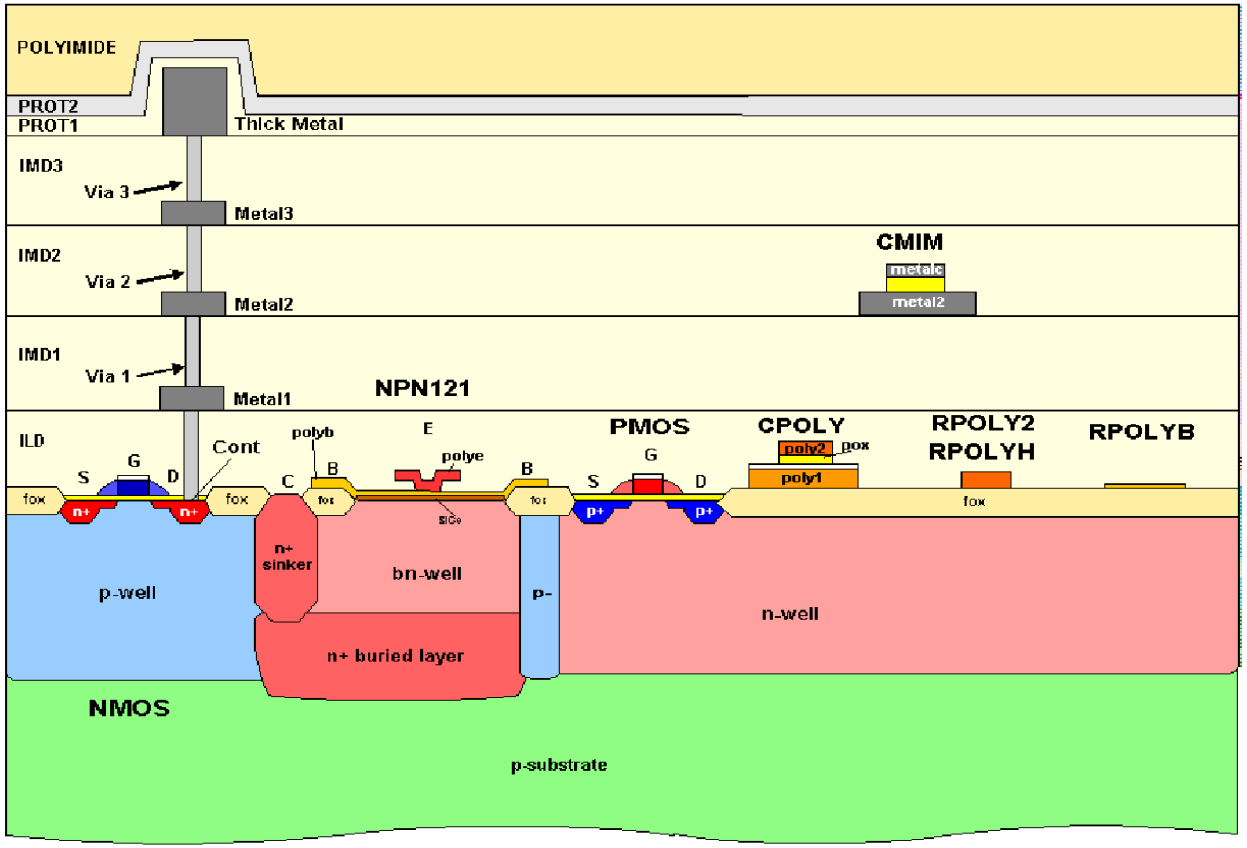
Cross-section of a photo-diode (BARC process option)

- **6 MPW runs scheduled in 2017.**
- **MPW Price : 650 Euro/mm² + fixed price of 6'900 Euro**

Process (0.35µ SiGe)

SiGe HBT-BiCMOS 0.35 µ S35D4M5

- 4 Layers Polysilicon / 4 Layers Metal.
- Power supply voltage range (2.5V – 3.6V / 5.5V)
- Vertical SiGe-HBT NPN : Ft = 70 GHz
- High Resistive Polysilicon.
- Poly1/Poly2 capacitors
- MIM capacitors
- Thick Top Metal



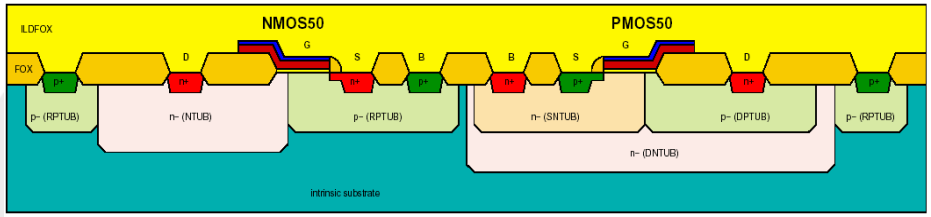
- **4 MPW runs scheduled in 2017.**
- **MPW Price : 950 Euro/mm²**

ams Process (0.35µ HV-CMOS)

HV CMOS 0.35 µ **H35 (H35B4D3)**

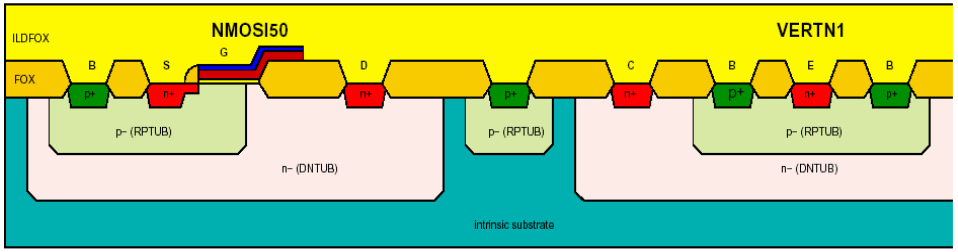
- 2 Layers Polysilicon, 4 Layers Metal, High Resistive Poly, Thick 4th Metal.
- 20V / 50 V / 120 V Maximum operating voltage.
- 3.3V / 5.0V / 20V Maximum gate voltage.
- R_{on} = 0.11 Ohm mm² for HV-NMOS
- R_{on} = 0.29 Ohm mm² for HV-PMOS

- **4 MPW runs scheduled in 2017.**
- **MPW New Price : 850 Euro/mm²**



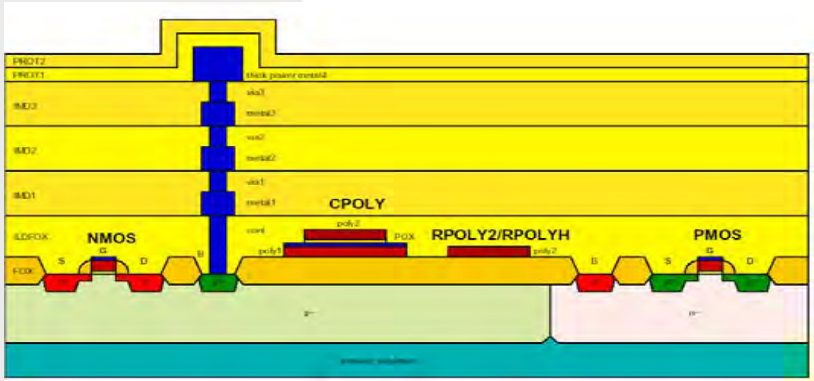
NMOS50 (50V)
NMOS120 (120V)

PMOS50 (50V)
PMOS120 (120V)



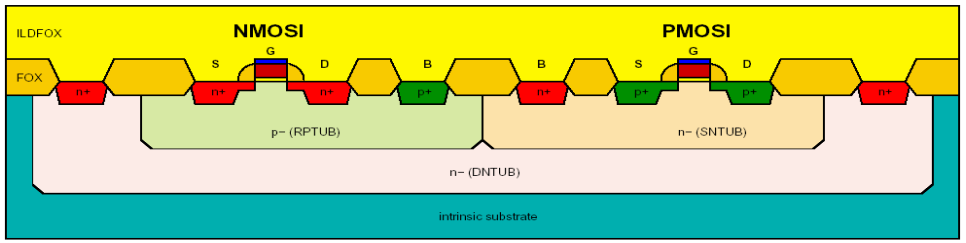
NMOSI50 (50V)

VERTN1



Standard 3.3V / 5V

Isolated 3.3V / 5V



0.18µ CMOS & High-Voltage CMOS

- CMOS technology with ≤ 3 mask level adders for HV
- Three gate oxides available: 1.8, 5V and 20V
- 6 metal levels (last metal: 4 µm Al power metal)
- Full set of 20 V and 50 V LDMOS devices
- Low Rdson
  - < 14 mΩ*mm^2@30 V BVDSS
  - < 130 mΩ*mm^2@70 V BVDSS
- 1.8 V and 5 V floating logic (N/PFET)
- High-voltage vertical NPN & PNP bipolar transistors
- Isolated JFET
- High-voltage VN capacitors (20-50V)
- High voltage well based resistors
- 1 kV, 2 kV and 4 kV HBM ESD protection structures
- OTP (Efuse)
- Tool for safe operating area check (SOAC)

➢ 4 MPW runs scheduled in 2017.
➢ MPW Price : 1'200 Euro/mm^2

amn Runs in 2016

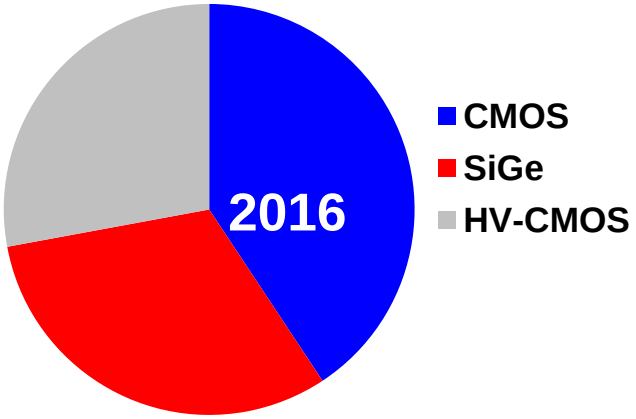
Number of prototypes in 2016 : 87 (83 in 2015)
Number of Low volume prod. in 2016 : 25 (25 in 2015)

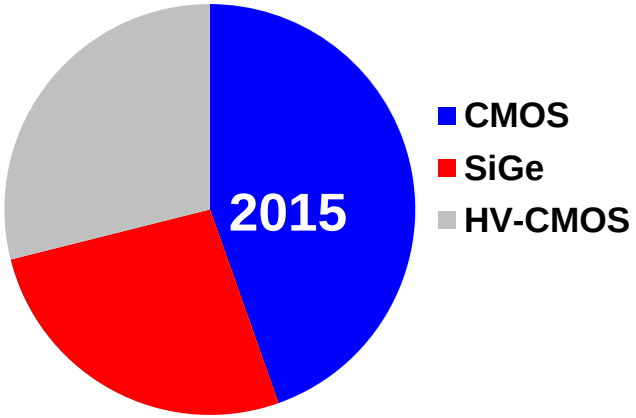
29 scheduled MPW runs (29 in 2015)
3 extra runs (Production) (1 in 2015)

35 circuits CMOS 40.2% (44.5% in 2015)
(37 in 2015)

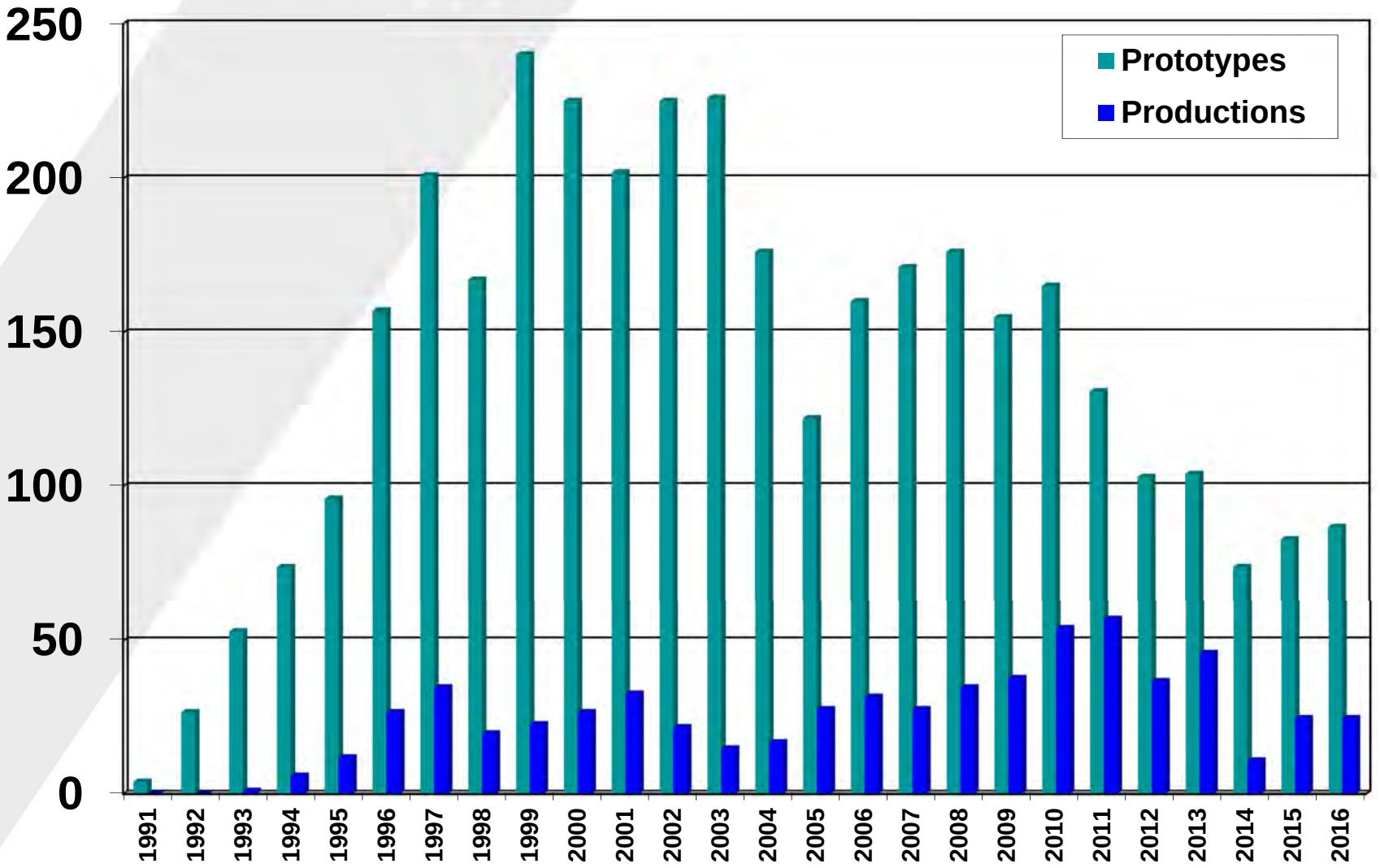
27 circuits SiGe 31% (26.5% in 2015)
(22 in 2015)

25 circuits HV-CMOS 28.8% (29% in 2015)
(24 in 2015)



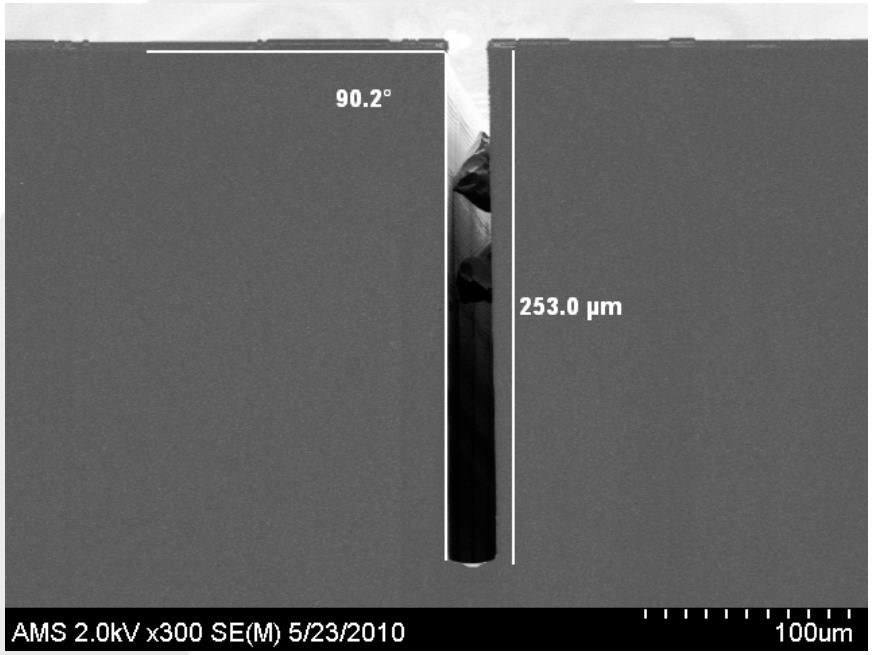


Runs Histogram



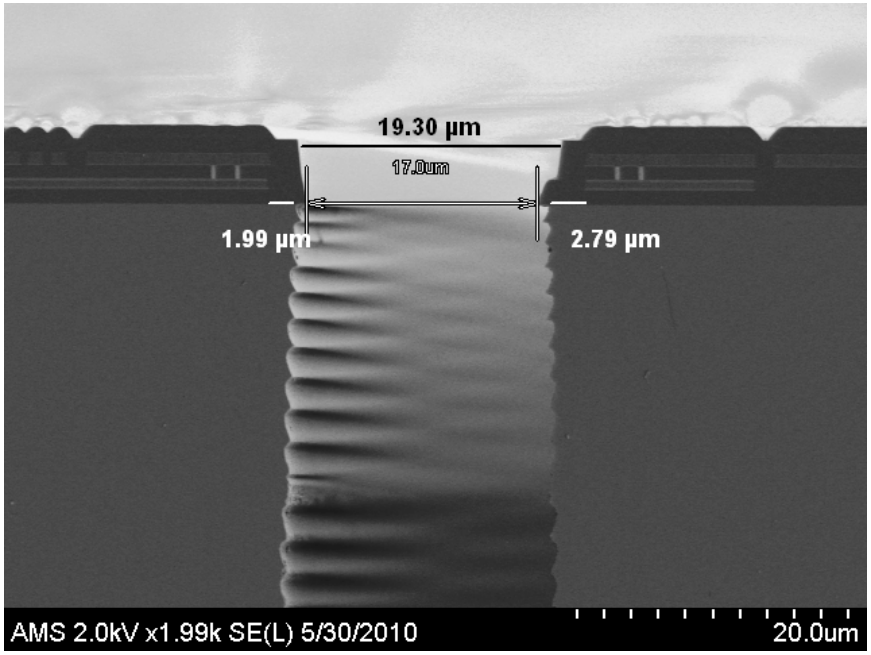
DRIE trench dicing at ams

Cross-sections: Width = 15µm, depth = 200µm



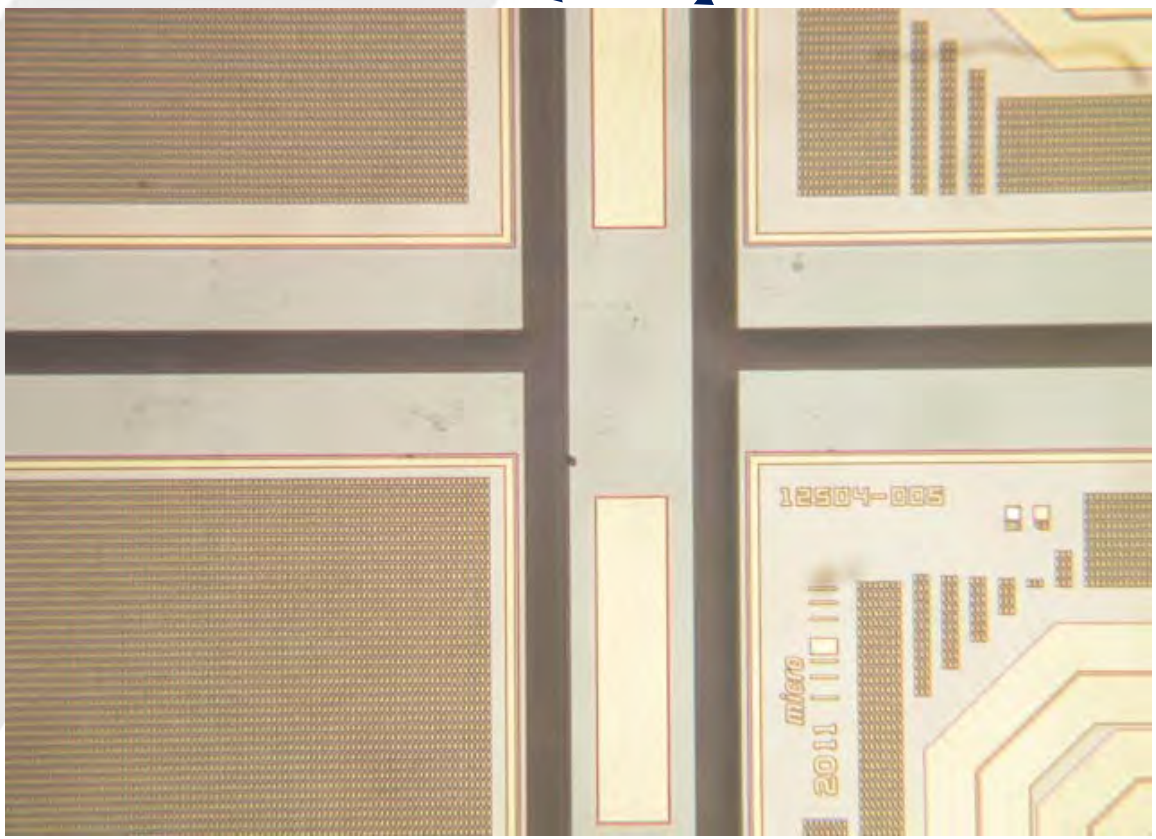
Trench 30um from edge: 90° / 253µm

(Courtesy AMS)



(Courtesy AMS)

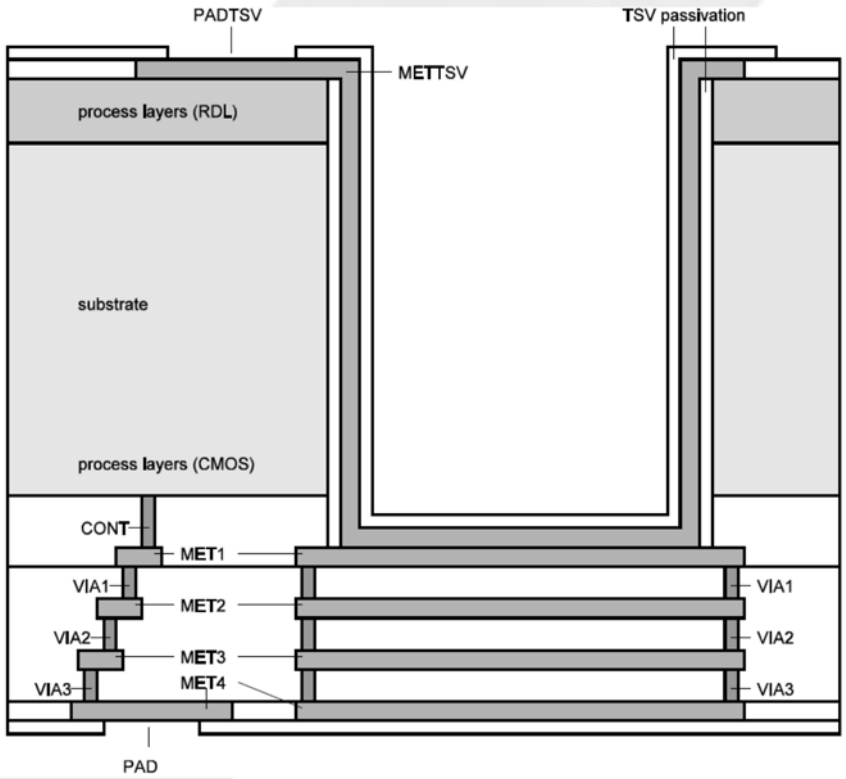
DRIE trench dicing at ams , cont'd



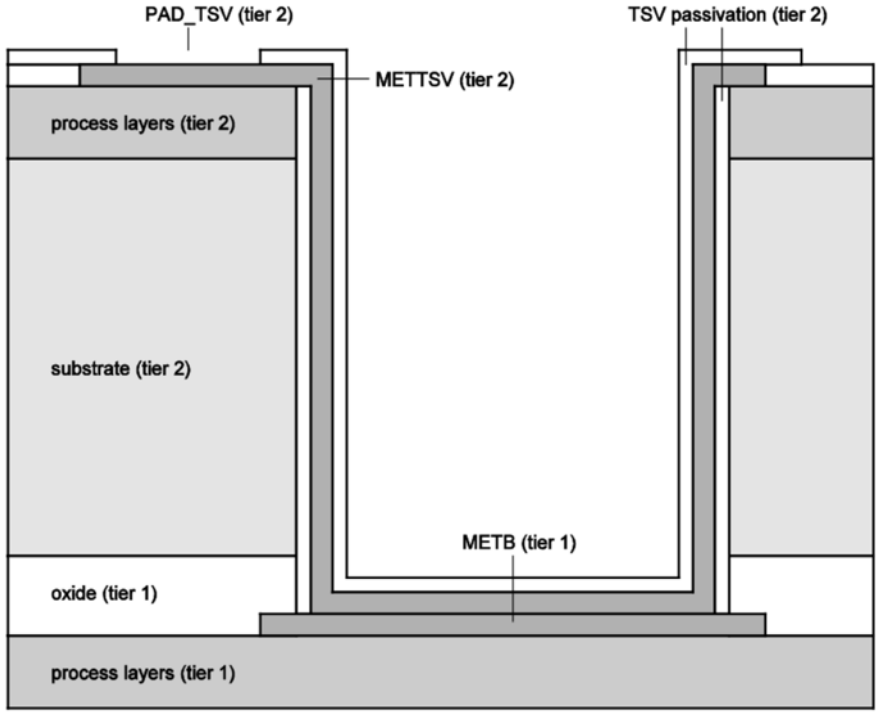
(Courtesy AMS)

- **Trench dicing available on request (one additional mask)**

TSV processes at ams



TSV on a single chip for backside bumping



Face2back two tiers stack. TSV on top tier's front side

- TSV post-processing available on dedicated engineering runs.
- UBM, RDL, and Bumping available on top of PADTSV.

Conclusion

- Comprehensive Process portfolio : CMOS, CMOS-Opto, CMOS-RF, SiGe, HV-CMOS, …
- New Pricing
- 6 MPW runs for 0.35um CMOS & CMOS Opto in 2017.
- 4 MPW runs for 0.18um CMOS / HV-CMOS, 0.35um SiGe, CMOS-RF, HV-CMOS
- Strong increase of parts quantities in low volume productions.
- Specific process options :
  - DRIE trench dicing
  - TSV : for single chip backside bumping or Face2back two tiers stacking
- Continuing the strong partnership and collaboration CMP / ams

http://cmp.imag.fr

web