MPW prices

Prices per mm² are for 25 bare dies except for MEMSCAP, Open 3D, Teledyne DALSA. Additional dies are charged.

DRC

Prices include DRC checking made by CMP before fabrication. In case of DRC errors CMP will contact you for corrections. Send your circuit layout before the deadline to have time for corrections.

Charged area

There is a minimum charge for each circuit depending on the technology considered for the design. This charge is defined as a minimum area. Excepted for MEMSCAP the charged area includes a seal ring of 60µm added by CMP around the circuit (120µm added in X and in Y axis).
For CMOS28nmFDSOI and for BiCMOS55 technologies, a discounted price per block has been defined. Blocks are 2 x 2mm² fixed sizes including a seal ring of 120µm. The effective design surface is therefore 1.88 x 1.88mm².

Examples for circuits in C35B4C3 technology of ams:

- The circuit size is 1500µm x 1600µm (dimensions withor without the seal ring), you are charged the minimum area, 3.43mm² (including seal-ring). 3.43mm² * 650€/mm² = 2230€.
- The circuit size is 3000µm x 3000µm (limit of pad ring), you are charged the following surface: (3000µm + 120µm)*(3000µm + 120µm) = 9.73mm². 9.73mm² * 650€/mm² = 6325€.

Additional circuits

Low volume (<100) of additional circuits can be ordered at any time as a function of availabilities. Larger volume (>300) of additional circuits must be ordered before the deadline for manufacture. Contact CMP for precise estimates. Prices are determined on a case per case basis.

Colour plots

Colour plots of the design can be ordered. Default format is around A0 (115cm x 76cm). Price: 40€ for the first sample and 25€ per copy.

Shipment fees

Depending on destination, shipment fees for circuits and packaging are charged from 60€ up to 350€. For packaging services out a regular MPW (=external project or new packaging request on existing dies) shipment fees to and from packaging subcontractors are applied.

Prices are exclusive of taxes and duties and can be changed at any time without prior notice.

CMOS/BiCMOS/SiGe Integrated Circuits

ams(1)			
	ams 0.18µm CMOS C18A6	1200€/mm² (2) 12000€ + [(Area-10) x 1100€]	*if Area less or equal to 10mm²* *if Area > 10mm²*
	ams 0.18µm HV-CMOS H18A6	1200€/mm² (2) 12000€ + [(Area-10) x 1100€]	*if Area less or equal to 10mm²* *if Area > 10mm²*
	ams 0.35µm CMOS C35B4C3	650€/mm² (3) 6500€ + [(Area-10) x 550€]	*if Area less or equal to 10mm²* *if Area > 10mm²*
	ams 0.35µm CMOS-RF C35B4M3	950€/mm² (4) 9500€ + [(Area-10) x 850€]	*if Area less or equal to 10mm²* *if Area > 10mm²*
	ams 0.35µm CMOS-Opto BARC C35B40A	650€/mm² (3) 6500€ + [(Area-10) x 550€] + fixed fee 6900€	*if Area less or equal to 10mm²* *if Area > 10mm²*
	ams 0.35µm CMOS-Opto ARC C35B4O1	700€/mm² (3) 7000€ + [(Area-10) x 600€]	*if Area less or equal to 10mm²* *if Area > 10mm²*
	ams 0.35µm SiGe BiCMOS S35D4M5	950€/mm² (4) 9500€ + [(Area-10) x 850€]	*if Area less or equal to 10mm²* *if Area > 10mm²*
	ams 0.35µm C35B4E3	Available upon request with additional fees.	
	ams 0.35µm HV-CMOS H35B4D3	850€/mm² (5) 8500€ + [(Area-10) x 750€]	*if Area less or equal to 10mm²* *if Area > 10mm²*
	ams 0.35µm MEMS Bulk -CMOS Bulk Micromachining front-side -CMOS Bulk Micromachining back-side	650€/mm² (4) + 3700€ for 10 dies price under request	
STMicroelectronics(1)			
	ST 28nm FDSOI CMOS28FDSOI	12500€/mm² (6) Special price for CNRS Institutions: 9850€/mm² (6) 39400€/block -> Each block is 2x2mm² (including seal-ring: effective design surface: 1.88 x 1.88mm²).	
	ST 55nm SiGe BiCMOS055	7900€/mm2 (6)if Area less or equal to 4mm² 25600€/block -> Each block is 2x2mm² (including seal-ring: effective design dimension:1,88x1,88mm²).	
	ST 65nm CMOS CMOS065	6500€/mm²(6) 32500€ + [(Area-5) x 5200€]	*if Area less or equal to 5mm²* *if 5mm² < Area < 15mm²(7)*
	ST 130nm CMOS HCMOS9GP	2500€/mm²(6) 12500€ + [(Area-5) x 2200€]	*if Area less or equal to 5mm²* *if 5mm² < Area < 15mm² (7)*
	ST 130nm SiGe BiCMOS9MW	3100€/mm²(6) 15500€ + [(Area-5) x 2600€]	*if Area less or equal to 5mm²* *if 5mm² < Area < 15mm² (7)*
	ST 130nm SOI H9SOI-FEM	2400€/mm² (6) 12000€ + [(Area-5) x 2000€]	*if Area less or equal to 5mm²* *if 5mm² < Area < 15mm² (7)*
	ST 130nm CMOS HCMOS9A	2500€/mm² (6) 12500€ + [(Area-5) x 2200€]	*if Area less or equal to 5mm²* *if 5mm² < Area < 15mm² (7)*
	ST 0.16µm BCD BCD8sP	2800€/mm²(20) 14000€ + [(Area-5) x 2300€]	*if Area less or equal to 5mm²* *if 5mm² < Area < 15mm² (7)*
	ST 0.16µm BCD BCD8sP-SOI	2800€/mm²(20) 14000€ + [(Area-5) x 2300€]	*if Area less or equal to 5mm²* *if 5mm² < Area < 15mm² (7)*

Silicon Photonic Integrated Circuits

new	**IRT Nanoelec - LETI-CEA**		
	Si310-PHMP2M	3200€/block ->Each block is 2x1mm² or 1x2mm² (1) (18) *if Area less or equal to 20mm² and* 2000€/block ->Each block is 2x1mm² or 1x2mm² (1) (19) *for additional blocks above 20mm².*	

Micro Electro Mechanical Systems - MEMS

	MEMSCAP		
	PolyMUMPs	3900€ (8) (9) (10) (13)	4600€ (11) (9) (10) (13)
	PiezoMUMPs	3900€ (8) (10) (13)	4600€ (11) (10) (13)
	SOIMUMPs	3900€ (8) (9) (10) (14)	4600€ (12) (9) (10) (14)

	Teledyne Dalsa		
	MIDIS	8000€ (4mm x 4mm) (8) (12) 15400€ (4mm x 8mm) (8) (12) 29800€ (8mm x 8mm) (8) (12)	9800€ (4mm x 4mm) (11) (12) 18700€ (4mm x 8mm) (11) (12) 37300€ (8mm x 8mm) (11) (12)

Advanced packaging

	OPEN 3D post process	
	Front-side: µ-Bumps or UBM (15) *Guaranteed minimum delivered pieces 40* *Applicable only on ams 0.35µm, ST 130nm, 65nm, 55nm and 28nm MPW for projects and wafers processed through CMP.*	22500€ + additional fees (16) (17) *Dedicated post process run: contact CMP*
	Back-side: TSV, RDL and Bumps (15) *Guaranteed minimum delivered pieces 40.* *Applicable only on ams 0.35µm, ST130nm, 65nm and 55nm MPW for projects and wafers processed through CMP.*	53500€ + additional fees (16) (17) *Dedicated post process run: contact CMP*
Open 3D-CMP post processes are available on the last MPW runs of the year for the following technologies: 0.35µm from ams, 130nm, 55nm, 65nm and 28 nm from STMicroelectronics.		

new	**ams 0.35µm Active Silicon Interposer with UBM**		
	3M+1TM** interposer *Guaranteed minimum delivered pieces 40*	50000€ *if Area < 100mm²* 64000€ *if Area < 100mm²*	
	ams 0.35µm Passive Silicon Interposer with UBM		
	3M+1TM** interposer (*Backend only*) *Guaranteed minimum delivered pieces 40*	40000€ *For Area >300 mm²: contact CMP*	

*** 3M+1TM: stack of 3 layers of metal and 4th Thick Top Metal.*

	ams Wafer-level packaging Bumps on any ams 0.35 and 0.18µm runs	
	ams Wafer-level bumping option	6200€ *per design for 25 delivered pieces*

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1. Area = (X + 0.12) * (Y + 0.12) mm².
2. Minimum charge is the price of 5.55 mm² (X+0.12)*(Y+0.12) mm².
3. Minimum charge is the price of 3.43 mm² (X+0.12)*(Y+0.12) mm².
4. Minimum charge is the price of 4.49 mm² (X+0.12)*(Y+0.12) mm².
5. Minimum charge is the price of 7.65 mm² (X+0.12)*(Y+0.12) mm².
6. Minimum charge is the price of 1.25 mm² (X+0.12)*(Y+0.12) mm².
7. Contact CMP for a price quotation when Area is larger.
8. Price for Educational Institutions and Research Labs.
9. Additional prices for Subdicing and Release:
   - Subdicing: 220€ per cut lane and per 15 chips,
   - HF Release: 870€ flat rate for up to 60 die/subdie,
   - Supercritical CO2 Dry: 1100€ flat rate for up to 60 die/subdie.
10. Contact CMP for multiple location prices.
11. Price for Industrial Companies.
12. Fixed size.
13. For 15 identical chips, 1cm x 1cm (fixed size).
14. For 15 identical chips 0.9cm x 0.9cm (fixed size).
15. OPEN 3D post-process MPW runs are subject to a sufficient level of participation.
16. Additional fees are applied function of the silicon MPW technology: 6.5k€ in 0.35µm ams/ 3.4k€ in 130nm STM/ 9k€ in 65nm STM/ 11k€ in 55nm STM / 13.5k€ in 28nm STM.
17. Option for flip chip assembly on provided substrates (max 50x50mm2): 5k€ for 40 pieces. For other request, please contact CMP.
18. Minimum charge is the price of 2 blocs or 4mm².
19. Minimum charge is 30000€.
20. Minimum charge is the price of 3.00 mm² (X+0.12)*(Y+0.12) mm².

Standard Packaging Information and Prices

Packaging is an important issue not to be neglected for the complete succes of a prototype production and implementation. The first step before starting a design is to select a package. Pad ring has to match with cavity of the selected package to optimize the whole interconnection. If the pad ring is not correct you will have to buy a dedicated package, this is time consuming and price can be significantly higher than price of silicon. General assembly rules and common errors are available on the web site.

A die ratio between 1 and 1.2 is recommanded. Packaging should be ordered via the CMP Order Form before the deadline of the run. The bonding diagram should be sent with the CMP Order Form. Please check on our website for technical constraints on pad ring and for the price list and possible additional fees.

Wire-bond packaging process flow for MPW runs

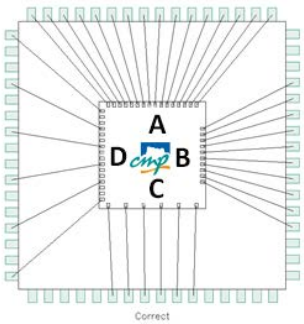
CMP offers a complete assembly service based on a wide range of ceramic and plastic packages for prototyping and low volume production.

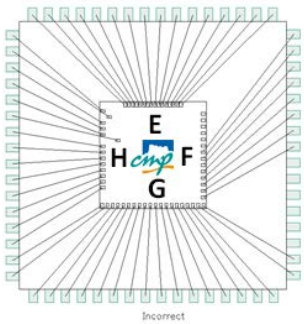
Packaging guidelines

Prototypes packaging is a hard issue and yield can't be guaranteed. The pad ring of the circuit have to match with the selected package to optimize the number of good samples. When you request bonding of additional circuits after runs you have to provide us with 5 additional dies for setup of the bonding machine. These dies can be damaged by setup.

At least the following simple rules have to be followed for prototypes in ceramic packages. They are not strong enough for low volume production:

- Bonding pads have to be connected to the side of the package that is facing.
- Use a homogenous spacing for pads with the first pad and the last pad near corners.
- Use the biggest width of bonding pad compatible with the number of pad in a side.
- All bonding pads should have the same size and are perfectly aligned along circuit edges.
- Bonding pad structure has to be strong enough to avoid stretch off when bonding wires.
- No bonding pad in corners.
- Avoid long wires. Check with us for wires longer than 4500µm.
- Angles of wires with the circuit edge have to be between 45° and 90°.
- A bonding wire can't cross another bonding wire (this generates a shortcut).





A: the best configurations.
B, C: good configurations when the number of pads is smaller.
D: dummy pads are correctly inserted.
E: pads are concentrated in the middle of the circuit's side.
F: dummy pads are concentrated on top (long wires and acute angles).
G: too many pads, pads in the corner, the 2 first pads and the 2 last pads are not connected to the package side that is facing.
H: pads are not aligned.

The diameter of wires used for a circuit depend on size of the smallest pad of the circuit and on type of bonding (ball bonding or wedge bonding).

Some factors that are reducing yield:

- Long wire (shorts with neighbouring wires or with package cavity)
- Small pads (thin diameter for wires, risk to stretch wires off pads)
- Acute angles between wire and circuit edge (< 45°, shorts)
- Pads not perfectly aligned along the circuit edge (shorts)
- Pads incorrectly distributed in a side of the circuit (shorts)
- Bad bonding-pad structure (pad destroyed by bonding)
- Bonding pads in corners (generation of cracks on die)
- Big circuit ratio, length/width > 1.8 (long wires + acute angles)

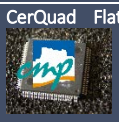
Available standard package types and associated services:

- A 200€ **wiring plan preparation fees** is applied for each packaging project + 100€ for each additional bonding diagram on the same die and package.
- A 200€ service fee is applied for **a new packaging request** of a previously processed project.
- An additional service fee is applied for packaging requests for IC **not fabricated through CMP**:
  - of 200€ for the first request,
  - of 100€ for each following request.

Depending on IC pad size, additional **set up fees** are invoiced:

- for 40µm to 50µm pad size: 400€
- for 51µm to 60µm pad size: 300€
- for 61µm to 75µm pad size: 200€
- for pads larger than 76µm no set up fees except for CQFPs and for QFNs packages: 200€

In all cases, **a minimum of five (5)** packages per bonding diagram has to be ordered.
Additional bonding wires can be charged. Price is quoted on a case per case basis for circuits with long wires.
For small volume packaging service, please contact us for a specific quotation.

Types & associated services		Relevant features	Price per unit	
Small Outline (SOIC) 	Ceramic		SOIC8: 67,90€ SOIC16: 69,90€ SOIC20: 80,60€	SOIC24: 83,80€ SOIC28: 87,50€
C-Leaded Chip Carriers (CLCC) 	Ceramic		CLCC16: 41,30€ CLCC20: 43,10€ CLCC28: 44,60€ CLCC32: 47,60€	CLCC44: 54,00€ CLCC48: 58,40€ CLCC68: 76,90€ CLCC84: 78,40€
J-Leaded Chip Carriers (JLCC) 	Ceramic/Plastic		JLCC28: 67,90€ JLCC44: 73,00€ JLCC52: 80,60€	JLCC68: 83,80€ JLCC84: 97,10€
Dual-in-line (DIL) 	Ceramic		DIL8: 31,90€ DIL14: 33,10€ DIL16: 34,40€ DIL18: 53,80€ DIL20: 36,90€	DIL24: 49,50€ DIL28: 53,60€ DIL40: 58,60€ DIL48: 63,50€
CerQuad Flat Pack (CQFP) 	Ceramic	Up to 256 I/Os Available options for pins: - Z: gull wing - J: Jleaded - F: Flat Default option is pins bent in gull wing	CQFP20J: 55,30€ CQFP44ZJF: 74,30€ CQFP64ZJF: 90,30€ CQFP68JF: 87,80€ CQFP80Z: 90,30€ CQFP84J: 91,50€ CQFP100ZF: 113,10€	CQFP120Z: 123,10€ CQFP128Z: 125,00€ CQFP144Z: 134,10€ CQFP160Z: 142,10€ CQFP208Z: 178,40€ CQFP240Z: 248,80€ CQFP256Z: 261,30€
Pin Grid Arrays (PGA) 	Ceramic	Up to 352 pins	PGA68: 69,90€ PGA84: 80,60€ PGA100: 95,30€ PGA120: 106,60€ PGA144: 115,50€	PGA160: 126,90€ PGA180: 138,50€ PGA208: 187,90€ PGA224: 223,40€ PGA256: 244,90€
Thin Quad Flat Pad (TQFP) 	Plastic open cavity	25 samples minimum Theses packages need thinned dies, lids must be sealed	TQFP32: 54,60€ TQFP44: 62,30€	TQFP52: 69,30€ TQFP64: 77,50€
Quad Flat Non Leaded (Open Cavity QFN) 	Plastic open cavity	Thermal performance, low inductance, high frequency Theses packages need thinned dies	QFN12: 45,80€ QFN16: 45,80€ QFN24: 58,40€ QFN28: 58,40€ QFN32: 68,60€ QFN36: 72,40€ QFN40: 73,00€	QFN44: 75,50€ QFN48: 77,50€ QFN52: 79,40€ QFN56: 82,50€ QFN64: 94,00€ QFN80: 105,40€
Plastic Open Cavity Packages 	Plastic	Allows a smooth transfer between ceramic and plastic pakage (QFN, QFP, PLCC, PGA, BGA)	*Upon request*	
Optical resin, Chip On Board (COB), Thermal solutions, Metallic & Hermetic package			*Upon request*	
Wafer level thinning		ams 0.35 µm (8"): standard thinning to 530µm ams 0.35 µm (8"): thinning to 250 µm on request STMicroelectronics 130 nm (8"): standard thinning to 375µm	Free of charge	
Die level thinning		Down to 150 µm (absolute limit 100µm)	Area<1mm²: 10€/die 1mm²<Area<5mm²: 13€/die 5mm²<Area<10mm²: 16€/die 10mm²<Area<15mm²: 20€/die 15mm²< Area contact CMP	
DRIE dicing	Option of thinning to 50µm	Clean borders of the chips, a better precision than conventional dicing	*Upon request*	

Notes: - Minimum charges apply on most MPW services (invoice of a minimum surface)
- Degressive prices are applied to most MPW service **- check on the web site –**
- Prices may change without notice.