From layout to chips

Please note... New URL: http://mycmp.fr

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Phone: +33 4 76 57 46 17
E-mail: cmp@mycmp.fr

Please note... new e-mail

ICs, Photonics, & MEMS Prototyping & Low Volume Production

Circuits Multi-Projets®

Multi-Project Circuits® (CMP) is a Multi-Project Wafer (**MPW**) service organization in Integrated Circuits (ICs), Photonic ICs and Micro Electro Mechanical Systems (MEMS) for prototyping and low volume production. Circuits are fabricated using industrial process lines for universities, research laboratories and industrial companies. Since 1981, 592 customers from 70 countries have been served, more than 7700 projects have been prototyped through 1029 runs and 70 different technologies have been interfaced.

CMP distributes Process Design-Kits (**PDK**) for CMOS/BiCMOS IC's, Photonic IC's or MEMS' technologies . Each of them contains technology files, simulation models, design rules, standard cell libraries of the chosen technology. A copy of any requested design kit can be sent to customer after a non-disclosure agreement (NDA) with CMP. Customer request and support are provided through our Web interfaces:

Design-Kit Request Form->http://cmp3.imag.fr/products/DK/dkr

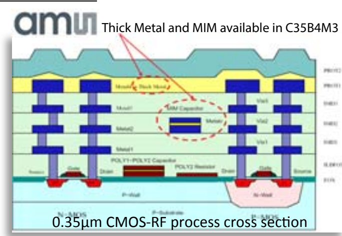
Design-Kit Support Center->https://cmp3.imag.fr/support

Please note... new e-mail

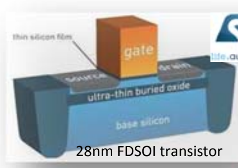
- Request Form: *Sylvaine EYRAUD [Sylvaine.Eyraud@mycmp.fr]*
- Support Center.: *Christelle RABACHE [Christelle.Rabache@mycmp.fr]*

CMOS/BiCMOS/SiGe Integrated Circuits*

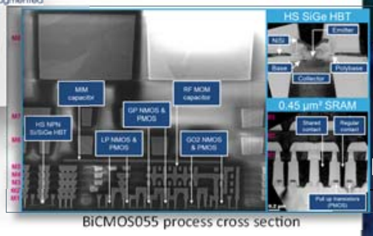
ams 0.18µm	*CMOS*	C18A6	1200€/mm²
	HV-CMOS	H18A6	1200€/mm²
ams 0.35µm	*CMOS*	C35B4C3	650€/mm²
	CMOS-RF	C35B4M3	950€/mm²
	SiGe BiCMOS	S35D4M5	950€/mm²
	CMOS-Opto BARC	C35B40A	650€/mm²+ fixed fee 6900€
	CMOS-Opto ARC	C35B401	700€/mm²
	HV-CMOS	H35B4D3	850€/mm²
ST 28nm	*FDSOI*	CMOS28FDSOI	12500€/mm²
ST 55nm	*SiGe*	BiCMOS055	7900 €/mm²
ST 65nm	*CMOS*	CMOS065	6500€/mm²
ST 130nm	*SiGe*	BiCMOS9MW	3100€/mm²
	CMOS	HCMOS9GP	2500€/mm²
	HV-CMOS	HCMOS9A	2500€/mm²
	SOI	H9SOI-FEM	2400€/mm²
ST 0.16µm	*BCD*	BCD8sP	2800€/mm²
new ST 0.16µm	*BCD-SOI*	BCD8sP-SOI	2800€/mm²



0.35µm CMOS-RF process cross section



28nm FDSOI transistor

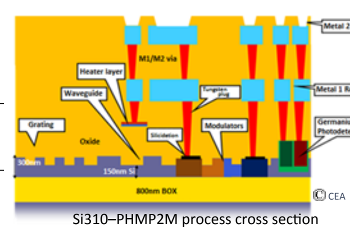


BiCMOS055 process cross section

Silicon Photonic Integrated Circuits*

IRT Nanoelec/LETI-CEA

	Si310–PHMP2M	1600€/mm²

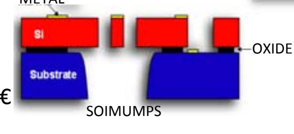


Si310–PHMP2M process cross section

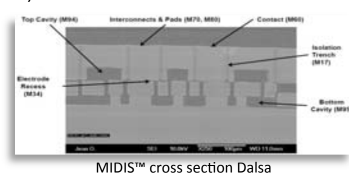
MEMS - Micro Electro Mechanical Systems -*

ams 0.35µm	*CMOS Bulk Micromachining front-side* 650€/mm² + 3700€ for 10 dies	
	CMOS Bulk Micromachining back-side price under request.	
MEMSCAP	*PolyMUMPs*	for 15 identical chips, 1cm x 1cm (fixed size) 3900€
	SOIMUMPS	for 15 identical chips, 0.9cm x 0.9cm (fixed size) 3900€
	PiezoMUMPs	for 15 identical chips, 1cm x 1cm (fixed size) 3900€
Teledyne DALSA	*MIDIS*	8000€ (4mm x 4mm)

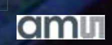
Silicon
Cross section Front-side Bulk

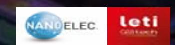


SOIMUMPS


MIDIS™ cross section Dalsa

Partnership:





June-17

Packaging

46, Avenue Félix Viallet
38000 Grenoble, France
Phone: +33 4 76 57 46 17
E-mail: cmp@mycmp.fr

Please note... new e-mail

CMP offers a wide variety of packages and assembly services.

⇒ *Before starting a design, an important step is to select a package: and/or package technic die-package compatibility optimization can significantly impact the overall system performances.*

Standard packaging

Complete assembly service based on a wide range of ceramic and plastic packages for prototyping and low volume production. Die pad ring compatibility with package cavity must be checked before sending your design.

Ceramic: *CQFP, DIL, LCC, JLCC, PGA, SOIC, QFN…*

Plastic: *BGA, QFN, QFP, PLCC, SOIC, TSSOP…*

Prices & guidelines available on the website.

Please note... new e-mail

Contact us
- Jean-Francois PAILLOTIN [Jean-Francois.Paillotin@mycmp.fr]
- Azedine MANAA [Azedine.Manaa@mycmp.fr]

Advanced packaging

Designers support every step of the way, from the 3D Add-on installation to the final assembly-level verifications of your 3D project, which requires a specific and individual follow-up.

OPEN 3D post-process in partnership with CEA/LETI in the frame of IRT Nanoelec

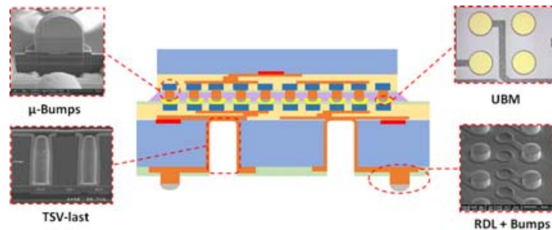
Set of post-processes allowing 3D interconnection integration at wafer-level, on various technology nodes after standard MPW & dedicated runs opened on STMicroelectronics **CMOS065, CMOS028FDSOI, BiCMOS055, BiCMOS9MW** & ams **C35B4M3.**

- ***Front-side modules:*** µ-Bumps / UBM
- ***Back-side modules:*** TSV last + RDL + Bumps

Various types of assemblies supported :

- Single Die bumping for ***Flip-Chip packaging***
- ***Die-to-die*** integration
- 2.5D integration on ***Silicon interposer***

40 pieces delivered, prices available on the website.

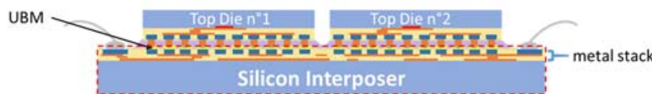


Silicon Interposer runs in partnership with ams and PacTech

2.5D Si-Interposer prototyping, including support for dedicated assembly as an option. Run opened once a year.

- Both ***active*** (Frontend + Backend) and ***passive*** (Backend only) runs are available
- Based on **ams C35** 4 layers metal stack (3 + 1 Thick)
- ***UBM*** deposited at (Ni/Pd/Au)

40 pieces delivered, prices available on the website.

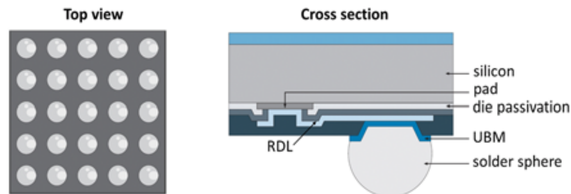


new **Wafer-level bumping** In partnership with ams

Wafer-level bumping service, manufactured on any ams 0.35 and 0.18µm runs. Supported in ams hitkit through an add-on.

- Evenly ***distributed array*** over chip surface
- Electrical connections to CMOS pads with ***RDL layer***
- I/O Pitch compatible ***PCB assembly processes***

Price available on the website.



Partnership:

Please note... new e-mail

Contact us
- Olivier GUILLER [olivier.guiller@mycmp.fr]
- Lyubomir KERACHEV [lyubomir.kerachev@mycmp.fr]

*Notes:
- Minimum charges apply on most MPW services (invoice of a minimum surface).
- Degressive prices are applied to most MPW service - check on the web site.
- Prices may change without notice.

May-17