



# ORDER FORM FOR ICs MANUFACTURING

CMP RUN:

TOPCELL NAME<sup>(1)</sup>:

PROCESS:

## DELIVERY & INVOICING

CIRCUIT'S PURPOSE:  Education  Research  Industry

INSTITUTION/COMPANY:

DELIVERY TO: Name:

Phone:

Institution/company:

Full address (no PO box):

SPECIAL REQUEST ON DELIVERY:  yes  no

*If no, circuits will be sent by courier service (UPS) with our standard 'invoice for customs' for foreign countries.*

INVOICE TO: Name:

Phone:

E-mail:

Institution/Company:

Address:

VAT id:

(Europe only)

P.O. number:

CIRCUIT SIZE: DeltaX ( $\mu\text{m}$ ) =

DeltaY ( $\mu\text{m}$ ) =

**NUMBER OF PARTS<sup>(2)</sup>** Bare dies: Packaged:

### **PACKAGE:**

Pad types:  wire bond  test probe  flip chip

Bonding diagram<sup>(3)</sup>:  free  imposed

ids:  removable  sealed

**BULK MICROMACHINING<sup>(4)</sup>**  yes  no

**COLOUR PLOTS:**  yes  no number:

**NON-STANDARD DIE THICKNESS<sup>(5)</sup>:**  $\mu$

**ADDITIONAL SERVICES<sup>(6)</sup>:**

### **Reserved to CMP**

area:

price

price

set\_up

price:

price

price

shipment:

**Total:**

*By signing the present order form, the responsible person accepts the Terms and Conditions that are in <http://mycmp.fr/services/terms-and-conditions.html>*

**Name and signature of the responsible person:**

Name:

date:

signature:



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## TECHNICAL INFORMATION

TECHNICAL ENQUIRIES<sup>(7)</sup>: Name:

Phone:

E-mail:

CIRCUIT TRANSFER:  web account (default)  ftp (files > 20MB)

DESCRIPTION FORMAT<sup>(8)</sup>:  GDSII Other:

CAD TOOL: version:

DESIGN KIT: version:

DRC VIOLATIONS:  yes  no *If you request DRC violations, please make a case overleaf.*

LIBRARY CELL REPLACEMENT REQUIRED<sup>(9)</sup>:  yes  no

*(make a list of used libraries)*

LIBRARY NAME

version

LOW VOLUME PRODUCTION EXPECTED?  yes  perhaps  no

VERSION OF DESIGN THAT SHOULD BE PRODUCED:  this one after test  an improved one

START PRODUCTION:  in next 6 months  < 1 year  > 1 year

EXPECTED NUMBER OF CIRCUITS:  < 100  < 1000  < 10000  > 10000

**CIRCUIT FUNCTION** *(a few lines in English. Mandatory for non E.U. countries, used for export regulation. Mandatory for technologies of STMicroelectronics. Will be published in the CMP annual report)*



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**DO NOT SEND THIS PAGE**

### RESERVATION REQUESTS

For technologies of STMicroelectronics you must send a reservation request **one month before the deadline**. Please contact us by Email for the document.

### PACKAGES

Packaging service is available if you are following packaging rules of CMP. Prices, list of packages and cavity maps are in:  
<http://mycmp.fr> -> Technologies -> Packaging  
<http://mycmp.fr> -> Technologies -> Price list -> CMP price list (right column)

Contact us for unlisted ceramic packages, we will check with our subcontractors.

Contact us for plastic packages. Small sets of plastic packages are possible. Main packages are SOIC, SSOP, LPCC (leadless), QFP, PLCC and EDQUAD (thermal solution).

**NB:** Design your pad ring according to the chosen package. Long wires and big angles are accepted for prototypes in ceramic packages and in open cavity packages but they are decreasing circuit performances. Packaging rules for plastic are strict for wire length and for angles of wires.

### NOTES

- (1) Maximum 14 characters, the first character must be a letter.
- (2) Default is 25 bare dies for our main technologies. Additional dies, color plots and packaging are charged.
- (3) Free means that CMP will make a bonding diagram and send it to you for approval. Note that CMP can't make bonding diagrams if the pad ring doesn't match with cavity of the selected package. If you send your bonding diagram please clearly identify pad #1 in your circuit.
- (4) Micromechanical systems are available only on ams 0.35µ technologies.
- (5) Standard die thicknesses (T) are as following. You can request another thickness for your application. Contact us for cost and delay. "T\*" means that die thickness can't be changed. Minimum thickness is 120µm for circuits smaller or equal to 3mm x 3mm.  
ams:                      0.35µ: T= 530µ      0.18µ: T= 530µ  
STMicroelectronics:   130nm: T= 375µ    65nm: T=250µ    55nm: T= 250µ    28nm: T=250µ    BCD8SP: T= 250µ
- (6) If you need any other service, contact us to check if we can provide it.
- (7) The person given on the form under the heading "TECHNICAL ENQUIRIES" must be rapidly available for questions and corrections of the design. The designer is generally the best choice.
- (8) For other format than gds2 contact CMP for an authorization.
- (9) Layout descriptions of library cells of STMicroelectronics contain only metal layers. For these technologies, library cells have to be replaced by the full layout version. **You must request replacement** and provide CMP with the list of used libraries and their versions.  
**NB: names of standard cells are reserved names. Using them for naming custom cell is forbidden otherwise custom cell will be overwritten by standard cell.**  
Example of request of "LIBRARY CELL REPLACEMENT" for a circuit in HCMOS9GP technology of STMicroelectronics:  
IOLIB\_65\_M6\_LL                      version 7.1  
COR9GPLL                              version 4.1  
DPHS9gp\_1024x32m16d4\_L        version DPHS\_180327