UTBB-FDSOI Design & Migration Methodology

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Central CAD & Design Solutions
• Introduction
• Digital design in UTBB FD-SOI
  • Standard Cells & Body biasing techniques
  • SRAMs
• Analog design in UTBB FD-SOI
  • Body bias generator
  • ESD & IOs
• Circuit porting experience
  • LDPC, MODAP examples
28nm Planar UTBB FD-SOI: Structure

Ultra Thin Body & BOX Fully Depleted SOI transistor
28nm Planar UTBB FD-SOI: Advantages

UTBB FD-SOI enables shorter channel length

• Ultra thin body
  • Better SCE immunity

• Ultra thin BOX
  • Extended body biasing

• Total dielectric isolation
  • Latch up immunity

• No channel doping
  • Improved variability

• Easy Porting from Bulk

UTBB FD-SOI enables shorter channel length

24nm

Hybrid zone

Body-Bias

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28FDSOI Process Flow at a Glance

**Caption:**
- Blue: Same as bulk
- Green: Adjustment vs bulk
- Red: New module
- Orange: Not use in FDSOI

**FEOL modules**
- STI module
- Wells i/i
- Hybrid block
- Ch. SiGe
- Vt Adjust
- Gate stack

**MEOL modules**
- Spacers
- Raised SD
- Junctions
- OP block
- Silicide
- Contact

**BEOL modules**
- M1 module
- Mx module
- M2x module
- MiM decap
- M8x module
- Far BEOL

-7 masks over 28LP Bulk Technology
Devices Partitioning in 28nm UTBB FD-SOI

<table>
<thead>
<tr>
<th>Device Type</th>
<th>UTBB FD-SOI</th>
<th>BULK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic</td>
<td>2Vt / PB0-16nm*</td>
<td></td>
</tr>
<tr>
<td>SRAM</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Capacitance, Varactor</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Drift MOS (OTP)</td>
<td>✓</td>
<td></td>
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<tr>
<td>Digital I/O</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Analog MOS</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>RF MOS</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Resistors</td>
<td>✓ (Poly)</td>
<td>✓ (Active)</td>
</tr>
<tr>
<td>Diodes (antenna)</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>ESD Devices</td>
<td>✓ (FET)</td>
<td>✓ (FET, diode, SCR)</td>
</tr>
<tr>
<td>Vertical Bipolar</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>

(*) **PB = Poly Bias**

28nm UTBB FD-SOI technology allows for modulating logic transistor effective gate length in the range 24-40nm for the authorized poly/contact pitch. The bias number (PB) indicates the additional value to the minimal length (24nm).

Key solutions for ESD protection & Performance enhancement
UTBB FD-SOI Design EcoSystem

- Planar UTBB FD-SOI uses a conventional (bulk) design flow
  - Cadence, Mentor, Synopsys,
  - Apache, Atrenta

- 4-terminals spice models available, derived from PSP
  - Major simulators supported
UTBB FD-SOI Specifics for power optimization

- Adaptive Voltage Scaling
- Dynamic Voltage & Frequency Scaling
- Power / Clock Gating
- Process Monitoring & Compensation
- Power Switches
- RTL Power Estimation
- Multi Vt Capabilities
- Reverse & Forward Body Bias
How to migrate Libraries on UTBB

- Full DP re-characterization with dedicated SOI models
  - Charac for various BB conditions depending on the performances targeted
- Retuning of limited number of critical IPs: Analog, IOs, Fuse
Standard cells & Body bias techniques
Stdcell Offer

- High Density (8T) and High Performance (12T)
- Dual VT: RVT and LVT.
- Multi Channel Length (Poly Bias) cells,
- Footprint compatible
Body Bias concept in UTBB FD-SOI

- No area penalty compared to Bulk
- Reuse of Bulk design techniques
- Speed/Power control

Back-gate contact
Body Bias: Speed/Power control

- Body Bias not degraded with scaling in FDSOI
- Body biasing fully inefficient in Finfet
Extended Body Bias Range in UTBB FD-SOI

Efficient knob for speed/leakage optimization

BULK

NMOS

UTBB FD-SOI

PMOS
UTBB FD-SOI: Extended Body Voltage Range

- Conventional Well (CW) - RBB

- Flip Well (FW) - FBB

Efficient knob for speed/leakage optimization

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UTBB FD-SOI: Constraints in RVT/LVT mixability

- **RVT: Conventional Well (CW)**
  - NMOS
  - PMOS
  - *Vddsp* and *Gndsn*

- **LVT: Flip Well (FW)**
  - NMOS
  - PMOS
  - *Gndsp*

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**Multi-Vt co-integration thanks to poly biasing**

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Extended Poly biasing in UTBB FD-SOI

- UTBB FD-SOI enables shorter channel length
- Enabling wider transistor effective gate length modulation

*From 24nm (PB0) up to 40nm (PB16)*

- CPP (Drawn) = 136 nm (relaxed, min is 126nm)

**Key solution for multi-VT & leakage optimization**
UTBB FD-SOI LVT [PB0-PB16] offers the same leakage range as RVT/LVT bulk flavors for better performances.

- 28nm Bulk at 1.0v, WC, -40c
- 28nm FDSOI at 0.85v, WC, 125c
Fine grain multi-\(V_T\) co-integration

RVT-like and SNW solutions enable multi-\(V_T\) like optimization
Single Well for Co-integration – “miX”-ing

- Standard RVT/LVT mimicked thanks to
  - Forward body biasing, width sizing or poly biasing

- Single Well ease the remapping from Bulk to SOI
  - More than 30% higher performance for the same leakage as bulk

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Porting methodology : Digital sections

RTL & PnR database (From Bulk)

RVT/LVT mixed in Bulk?

• Replace Libs
  • STA
  • ECO

N

Y

Std. Flow with one type:
• RTL Verif
• Synthesis
• Pnr
• STA

DRC + LVS + Extraction

Post Layout Verif
• PL Netlist + SDF + Sims

• AFE Block

TOP Integration & Checks

AMS Verification

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28nm UTBB-FDSOI SRAM
<table>
<thead>
<tr>
<th>Bit-cells</th>
<th>28LP</th>
<th>28FDSOI</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>D120 cell</strong></td>
<td>Gnds=0V Vdds=Vdd</td>
<td>FBBmax=0.3V RBBmax=0.3V</td>
<td>RVT</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Gnds=0V Vdds=0V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Body bias</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>FBBmax (V&gt;0)=0.3V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Full RBB (V&lt;0)</td>
</tr>
<tr>
<td><strong>B152 cell</strong></td>
<td>Gnds=0V Vdds=Vdd</td>
<td>FBBmax=0.3V RBBmax=0.3V</td>
<td>LVT (Flip-Well)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Gnds=0V Vdds=0V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Body Bias</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Full FBB (V&gt;0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RBBmax (V&lt;0)=−0.3V</td>
</tr>
<tr>
<td><strong>RF251 cell</strong></td>
<td>Gnds=0V Vdds=Vdd</td>
<td>FBBmax=0.3V RBBmax=0.3V</td>
<td>RP (RVT→LVT)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Gnds=0V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Full FBB (V&gt;0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RBBmax (V&lt;0)=−0.3V</td>
</tr>
<tr>
<td><strong>L197 cell</strong></td>
<td>Gnds=0V Vdds=Vdd</td>
<td>FBBmax=0.3V RBBmax=0.3V</td>
<td>Single-Well</td>
</tr>
<tr>
<td>(ST specific)</td>
<td></td>
<td></td>
<td>Gnds=0V Vdds=0V</td>
</tr>
</tbody>
</table>

---

**28FDSOI SRAM Offer**

- **D120 cell**: Gnds=0V, Vdds=Vdd, FBBmax=0.3V, RBBmax=0.3V.
- **B152 cell**: Gnds=0V, Vdds=Vdd, FBBmax=0.3V, RBBmax=0.3V.
- **RF251 cell**: Gnds=0V, Vdds=Vdd, FBBmax=0.3V, RBBmax=0.3V.
- **L197 cell** (ST specific): Gnds=0V, Vdds=Vdd, FBBmax=0.3V, RBBmax=0.3V.

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SRAM Vmin Comparison

![Graph showing Vddmin comparison between 28LP and 28FDSOI technologies.](image)
PPA with 28FDSOI at same voltage as 28Bulk

Timing: Bulk and SOI@Slow 0.9V -40C leakage/Dynamic power : Bulk / FDSOI@Fast 1.0V 125C

Access time reduction in FDSOI vs Bulk:
DPREG : -44% / SPHD : -43% / SPREG : -36%

Max frequency gain in FDSOI vs Bulk
DPREG : 65% / SPHD : 77% / SPREG : 75%

Leakage saving in FDSOI vs Bulk
DPREG : -29% / SPHD : -19% / SPREG : -40%

Dynamic power saving in FDSOI vs Bulk
DPREG : -13% / SPHD : -18% / SPREG : -14%

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28nm UTBB-FDSOI Analog design
Porting methodology: Analog sections

Schematic (From Bulk):
- RVT MOS: No Change
- LVT MOS: Bulk connection change
- CDM rules integration: Few changes in specific cases

Layout (From Bulk):
- Pcell based: Automatic hybrid addition
- Handcrafted: Manual Hybrid layer addition + Adjustment for spacing
- CDM & Antenna rules integration: S/D need antenna check

Layout:
- Clean DRC + LVS
- Extract Post layout netlist

Post Layout Tuning:
- Schematic + Layout
- LVS, DRC, Extraction

Characterization:
- Analog top simulations
- Timing Extraction

TO Integration & Digital Flow

~80% activity automated by PDK tools for Pcell based designs
PLLs porting example: Analog blocks

- **VCO** (current controlled ring oscillator based design)
  - Using thin oxide transistors (SG) for high speed requirement (few GHz).
  - Same current is kept in VCO to get same analog performances
    - No power gain in this specific stage

- **PFD** (Phase Frequency Detector) and **CP** (Charge Pump) are compatible with direct porting with minor manual retuning
  - Up to 60% leakage gain with UTBB EG (analog supply)
  - ~10% dynamic power gain (analog supply)

- **Bandgap: design retuning**
  - Performances are intimately dependent on PNP characteristics
  - A design update is needed here to restore identical performances in term of temperature control, PSRR, reference current spread and amplifier stability

Global PLL power status: 10-15% gain on dynamic and leakage powers
PLLs porting example: Digital blocks

- PLL is a mix of RVT and LVT blocks

- RVT blocks
  - UTBB FD-SOI RVT faster than bulk LP RVT
  - Used in small blocks having overall low leakage contribution
  - **Blind and fast porting** ⇒ Layout unchanged
  - ~10% gain on dynamic power, negligible PLL leakage variation

- LVT blocks
  - UTBB FD-SOI LVT much faster than bulk LP LVT but more leaking at constant definition
  - **25% leakage gain** by using speed/leakage tuning advantage of UTBB FD-SOI
    - Higher PB ⇒ Same performance ⇒ Reduced leakage
    - No Area Penalty since the gate sizing is done at constant overall device size
  - ~10% gain on dynamic power
Experience return for mixed signal IPs porting

• Low porting cycle time from 28nm LP to 28nm UTBB FD-SOI
  • ~3 months for complex IPs: LPDDR2 1066, PLLs up to 4.6Ghz, D-PHY 1Gbps
  • …against ~twice effort when doing standard porting from Bulk to Bulk
  • Leveraging on
    • Higher performances of UTBB devices
    • Layout compatibility with existing areas in Bulk
    • Automatic porting tools from PDK managing ~80% of activity to get DRC/LVS clean

• Porting from bulk using same design environment, at constant abstract
  • Secure concurrent development of whole SoC

• UTBB FD-SOI devices offering finer granularity in performance optimization
  • 2 Vt for thin and thick oxyde transistors
  • Each Vt covering wider range of speed and leakage (LVT leakage tuning over 30x range)

• Power saving
  • Digital blocks of IPs: ~25% leakage power gain ; ~10% dynamic power gain
  • Analog blocks of IPs: no generic value, depends on feature/performance specificity
Body-Bias Generator
Body-Bias voltages generation

• How to generate programmable body voltages?

![Diagram of Body-Bias voltages generation](image)
Output Amplifiers design

- AB-class for fast transients
- Symmetrical outputs
- Low Vt PMOS
- Ultra-low Vt NMOS (full FBB)

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### BBGEN ID card

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size (µm)</td>
<td>400x800</td>
</tr>
<tr>
<td>Vbbp range</td>
<td>0 → -1300mV</td>
</tr>
<tr>
<td>Vbben range</td>
<td>0 → 1300mV</td>
</tr>
<tr>
<td>Settling time 0→1300mV</td>
<td>1.3µs @ max load</td>
</tr>
<tr>
<td>Quiescent current</td>
<td>4mA typ</td>
</tr>
<tr>
<td>Load range</td>
<td>1-20 nF + 10Ω min ESR</td>
</tr>
<tr>
<td>Techno Options</td>
<td>None</td>
</tr>
<tr>
<td>BEOL</td>
<td>10ML</td>
</tr>
<tr>
<td>Supply</td>
<td>1.8V</td>
</tr>
<tr>
<td>Ext cap</td>
<td>1µF</td>
</tr>
</tbody>
</table>

Charge pump
ESD & IO Strategy in UTBB FD-SOI
Objectives

• Understand specific Fully-Depleted SOI (FDSOI) technology constraints for the ESD designer

• Discuss ESD devices placement to reach the optimum ESD performance

• Demonstrate the efficiency of Hybrid Bulk/FDSOI co-integration to design ESD networks
ESD devices placement rules (1 of 4)

- **STI Diode**
  - Not optimal due to high forward recovery time...
  - …but very high voltage tolerance
  - Shallow BOX kills the diode → Hybrid Bulk only

- **Gated Diode**
  - Surface conduction makes it very efficient
  - Diode architecture also compatible with BOX
  → Hybrid Bulk OR Thin Film
ESD devices placement rules (2 of 4)

- **NFET operated as BigFET ESD Clamp**
  - Operates in linear regime, no self-heating & BJT
  - Thin Film to benefit from better NFET perf. and body biasing features

- **MOS capacitance used for RC trigger circuit**
  - Abrupt decrease in moderate inversion (FDSOI)
ESD devices placement rules (3 of 4)

- **Un-silicided ESD FETs used as lateral bipolars**
  - GGNMOS Lateral bipolar conduction compatible with both Hybrid Bulk and Thin Film but…

<table>
<thead>
<tr>
<th></th>
<th>Hybrid</th>
<th>Thin Film</th>
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<tbody>
<tr>
<td><strong>Layout compatibility</strong></td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td><strong>Maximum ESD current</strong></td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td><strong>Triggering voltage</strong></td>
<td>- (High)</td>
<td>+ (Low)</td>
</tr>
</tbody>
</table>

Diagram:
- Vdd
- IO
- Gnd
- Hybrid
- FDSOI

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ESD devices placement rules (4 of 4)

- How to protect thin film designs with Hybrid ESD devices?
  - Innovative BIMOS concept in Hybrid Bulk

- Triggering voltage tuned by external resistance
- Same High current performance than GGNMOS
ESD FETs: Hybrid vs Thin Film

- **Silicon results**: TLP(100ns) performance comparison
Gated diodes: Hybrid vs Thin Film

- **Silicon results**: (vf) TLP performance comparison

![Graph showing comparison between Hybrid Bulk and FDSOI diodes](image)

- **HYBRID BULK**

- **FDSOI**

- 9 ns
- 100 ns

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ESD clamp

- SPICE comparison of different design scenarios.

<table>
<thead>
<tr>
<th>Design Scenario</th>
<th>Leakage @Vdd</th>
<th>$V_{\text{overshoot}}$ <em>(2kV HBM)</em></th>
<th>$V_{\text{max}}$ <em>(2kV HBM)</em></th>
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</thead>
<tbody>
<tr>
<td>Reference = Bulk 28LP (clamp pwell@GND)</td>
<td>48nA</td>
<td>1.4V</td>
<td>1.5V</td>
</tr>
<tr>
<td>FDSOI/porting (Bulk direct porting)</td>
<td>4nA</td>
<td>1.4V</td>
<td>1.5V</td>
</tr>
<tr>
<td>FDSOI/boosted (dynamic body biasing) **</td>
<td>4nA</td>
<td>1.1V</td>
<td>1.3V</td>
</tr>
<tr>
<td>FDSOI/boosted_LVT (dynamic body biasing + ground plane swap) **</td>
<td>40nA</td>
<td>0.9V</td>
<td>1.15V</td>
</tr>
</tbody>
</table>

*23%*
Standalone supply clamp analysis

- 40µm width IO power cell: ESD devices split

RC triggered BigFET + reverse diode

Secondary protection for non-calibrated ESD
Application to the ESD remote network

- **FDSOI/boosted_LVT** design allows a **30% clamp width reduction** wrt 28LP Bulk design
  
  - similar clamp placement rules with smaller clamp

\[1\text{mm}(28\text{LP Bulk}) \rightarrow 1.5\text{mm}(28\text{nm FDSOI})\]
FDSOI is latch-up free

- Remaining Injectors in Hybrid zones (mainly ESD devices).
  - LU between Hybrid parts.
  - LU due to abutment between IO Pad and Wells (especially if NW@0V)

- Reduced set of LU rules apply on Hybrid zones
Process induced damage in FDSOI

• In Bulk technology, Gates are isolated from the substrate → antenna rules to protect gates

• In SOI technology, both Gates and SD are isolated from the substrate → antenna rules to protect gates and SD
• ESD strategy is portable from Bulk to UTBB FD-SOI using Hybrid area

**Advanced ESD Strategy**
- Distributed ESD clamps
- Fully predictable by Spice simulations
- Elementary devices UTBB silicon validated

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Minimum Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD Voltage Protection</td>
<td>HBM</td>
<td>2kV</td>
</tr>
<tr>
<td></td>
<td>MM</td>
<td>100V</td>
</tr>
<tr>
<td></td>
<td>CDM</td>
<td>500V</td>
</tr>
<tr>
<td>Injection current</td>
<td>Ambient temperature</td>
<td>200mA</td>
</tr>
<tr>
<td></td>
<td>80°C</td>
<td>100mA</td>
</tr>
</tbody>
</table>
Bulk to UTBB-FDSOI: Circuit portability experience
## UTBB FDSOI: Proof of concept

<table>
<thead>
<tr>
<th>BULK LIKE</th>
<th>UTBB FD-SOI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design:</td>
<td>Design:</td>
</tr>
<tr>
<td>Conv. Well</td>
<td>Flip Well</td>
</tr>
</tbody>
</table>

### Technologies
- 28nm LP FDSOI & BULK

### Transistors
- 150 Million RVT, LVT, EG

### Interconnect
- 7 Cu Metal + AL RDL

### Die size
- 10mm²

### LDPC core
- 0.25mm²

### Vdd
- [0.35V; 1.5 V]

### Vbb
- [-1V ; 1V]
UTBB FD-SOI Max Frequency vs. BULK

Wide operating range 6MHz/0.35V to 525MHz/1.5V

LDPC 6T-SRAM (FBB 1V) functional down to 0.41V
UTBB FD-SOI Total Power vs. BULK

- Vdd: 0.6V to 1.5V step 100mV
- FBB=0.3V, FBB=1V, noBB
- +35% increase, -49% decrease
- BULK-LP, UTBB FD-SOI
UTBB FD-SOI Leakage Power vs. BULK

Wide body-bias modulation: 10X leakage benefit

Vdd=0.6V

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UTBB FD-SOI Energy Efficiency vs. BULK

Vdd: 1.5V to 0.6V step 100mV

(1V, 0.3V) => Ref
(0.8V, 0V) => -34%
(0.7V, 1V) => -50%

50% EDP savings thanks to (Vdd, Vbb) modulation

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Half Node Effort for Full Node Benefit

L8580
Combining Performance Boost with Best in Class Power Efficiency

Optimized Solution for Smartphones
- 28nm Single Chip LTE modem & Dual Core Application Processor @ 2.3GHz
- Best in class Low Power operation, 31DMIP/mW @ 0.6V
- Linux BSP for Android / Windows Phone 8
- Full set of connectivity

Mobile Broadband Everywhere
- 3GPP Rel. 8/9, LTE 100/50 Mbps, CA, HSPA+ 84/11 Mbps with MIMO and dual-cell capabilities
- TD-LTE/TD-SCDMA for Chinese market
- Worldwide coverage with up to 9 bands in one device
- Fully Leverage M7400 stand-alone LTE modem certification & deployment

Great User Experience
- High performance system thanks to Dual 32bits LPDDR2 @ 533MHz support
- High quality 300dpi 4.5” HD display support
- Advanced 3D UI & Gaming with 1.2Gpx/s, 105Mtr/s & 22Gflops GPU
- Multi standard 1080p video codec’s enabling Blue-Ray quality video

DB8580

- Video
- ARM® Cortex
- Imaging
- ISP
- Display
- Composition
- Peripherals
- Graphics
- IMG SGX544-MP1

28LP PG wk1229 FO wk1244
28FD PG wk1235 FO wk1243
Android booting wk1246
CES show 2.8GHz + 0.63V/1GHz wk1302

STMicroelectronics

STerminated CErs

L8580

STerminated CErs

Synopsys

Synopsys

28nm Single Chip LTE modem & Dual Core Application Processor @ 2.3GHz
Best in class Low Power operation, 31DMIP/mW @ 0.6V
Linux BSP for Android / Windows Phone 8
Full set of connectivity

3GPP Rel. 8/9, LTE 100/50 Mbps, CA, HSPA+ 84/11 Mbps with MIMO and dual-cell capabilities
TD-LTE/TD-SCDMA for Chinese market
Worldwide coverage with up to 9 bands in one device
Fully Leverage M7400 stand-alone LTE modem certification & deployment

High performance system thanks to Dual 32bits LPDDR2 @ 533MHz support
High quality 300dpi 4.5” HD display support
Advanced 3D UI & Gaming with 1.2Gpx/s, 105Mtr/s & 22Gflops GPU
Multi standard 1080p video codec’s enabling Blue-Ray quality video

Android booting wk1246

CES show 2.8GHz + 0.63V/1GHz wk1302
UTBB FD-SOI SOC implementation experience

• Same design flow as for 28nm LP
  • Same tools used
  • Same design cycle time

• For porting, used direct mapping of IPs + ECO
  • Script based
  • Faster than rerunning synthesis
  • Floorplan reuse

SOC in UTBB FD-SOI design effort is equivalent to a half node migration
### UTBB FD-SOI key techniques for SOC implementation

#### CPU:

<table>
<thead>
<tr>
<th>Techniques</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Flip Well implementation</td>
<td>• Increased peak performance</td>
</tr>
<tr>
<td>High performance L1Cache – 3GHz+</td>
<td>• Increased energy efficiency</td>
</tr>
<tr>
<td>Multi OPP implementation</td>
<td>• Reduced leakage in idle mode</td>
</tr>
<tr>
<td>Aggressive body biasing</td>
<td></td>
</tr>
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</table>

#### Other SOC IPs

<table>
<thead>
<tr>
<th>Techniques</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full RVT implementation</td>
<td>• Fast execution</td>
</tr>
<tr>
<td>Straightforward remapping from bulk</td>
<td>• Reduced dynamic power</td>
</tr>
<tr>
<td>Reduced power supply</td>
<td>• Reduced leakage in idle mode</td>
</tr>
</tbody>
</table>
Dynamic Process Scaling (Body Bias) Advantage

- **Same Perfs as 28LP with 200mV Less**
- **-400mV with 1.3V FBB**

- **Hit 3GHz Target**

- **>80% extra speed @ 1.3V FBB**
- **1GHz with FD-SOI**

28nm planar UTBB FD-SOI

Sept 13
Conclusion

• Breakthrough technology customers seeking a power/performance advantage

• UTBB libraries and I ps can be easily derived from Bulk

• Body Biasing techniques in UTBB-FDSOI
  • Key solution for high performance/low power application

• Best Speed / Power performances ever
  • Full Flexibility to cover full spectrum from LP to HP

• UTBB Credible alternative to FinFET
Acknowledgements

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• CCDS & STD teams from STMicroelectronics
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