

The NCSU Tezzaron Design Kit

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November 18, 2010

Outline

- ▷ **NCSU Design Kit “User Guide”**
- ▷ **Verilog Memory Model**
- ▷ **Lessons learned in assembling the reticle**

NCSU TDK overview

▷ Cadence

- ◆ You must use a version of Cadence that can understand Opus database libraries. (i.e. pre-6.0)

▷ Technology files

- ◆ The Chartered chrt013lp technology library was slightly modified to align the layer numbers with the R3logic technology library, which was the official library for the first MPW run. chrt013lp was used exclusively as the rf technology file was initially identical.

▷ DRC

- ◆ 2D DRC using Chartered DRC deck on each tier
- ◆ 3D DRC using Tezzaron 3D deck on each tier

▷ LVS

- ◆ Full 3D LVS is provided using one of two available simple LVS flows

Installation

▷ Installation is simple but there are two caveats

- ◆ We assume you are running tcsh or csh. If you aren't, you can easily get them from <http://directory.fsf.org>, and they install in about 5 minutes.
- ◆ You need to have gnu sed. The sed that comes with SunOs doesn't work. Fix: 5 min. <http://directory.fsf.org> sed from any Linux distro will be fine.

▷ Typical installation process:

- ◆ `gunzip chrt13lprf_DK009_Rev_1C_TSC.tar.gz`
- ◆ `cd chrt13lprf_DK009_Rev_1C_TSC_1C`
- ◆ `./install.sh`

Using the kit with Cadence

- ▶ **Main issue is you need the TDK's .cdsinit file in your working directory.**
- ▶ **You will also need to have at least some lines from the cds.lib file in your working directory's cds.lib file.**
- ▶ **The kit's cds.lib file assumes you have set the environment variable CDSHOME to point to your Cadence installation directory. See top-level README file for details.**
- ▶ **The add_TDK file can be sourced to make startup easier. See top-level README for details.**

DRC

▷ DRC is straightforward.

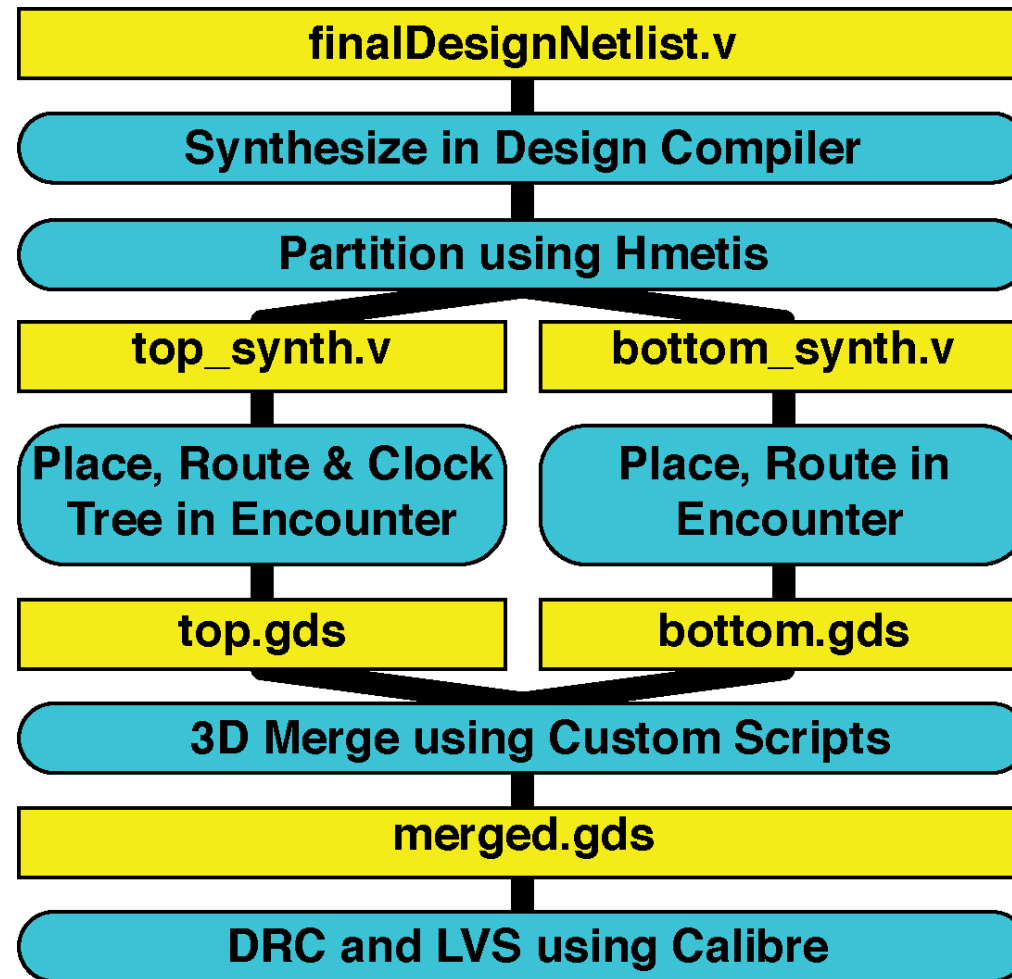
- ◆ If you do the installation as described in the top-level README file, the correct Chartered 2D DRC deck should be automatically selected from Calibre menu in icfb. See top-level README if it doesn't work out of the box.
- ◆ To do 3D DRC you will need to change the DRC Rules File entry under the Rules tab of the Calibre Interactive dialog box to point to `drc_header_1p_00_3D` in the `3DDRC` directory.
- ◆ Please note that the kit assumes that your Calibre installation works like the one at NCSU, which provides an environment variable named `MGC_HOME`. If it doesn't, you will have to provide one pointing to your Mentor Graphics (calibre) installation directory.

LVS

▷ There are two flows for doing full 3D LVS:

- ◆ Simplest flow:
 - ◇ Draw 1 schematic covering both tiers, layout each tier in it's own top-level cell, say tier0 and tier1
 - ◇ Run mpwMergeTiers script to combine layouts
 - ◇ Use our 3D LVS deck in Calibre
- ◆ Flow if using Encounter/Verilog/etc:
 - ◇ Generate layouts using Encounter (Design->Save->GDS)
 - ◇ Use our gdsmerge command to combine layouts
 - ◇ Use v2lvs to create netlist
 - ◇ Use our 3D LVS deck in Calibre
- ◆ Full details in doc/3DLVS.readme, including an example of the first flow with all files needed in the kit.

NCSU SAR Toolflow used for MPW



Important lessons from MPW1

- ▷ **The guard ring was a killer. Have everyone use a guard ring that you know is proven correct from the beginning.**
- ▷ **3DDRC: Do 3DDRC early and often. Confusion caused some MPW1 groups not to run 3D DRC until the last minute causing big trouble.**
- ▷ **Don't put shapes on label layers! The DRC/LVS decks will consider them conductors and hook up things that aren't really hooked up!**
- ▷ **Fill:**
 - ◆ Some tools, like memory generators, create large shapes on layer 252: NOFILL which you don't want.
 - ◆ Only use fill deck in FILLDRC directory.

Tezzaron Memory Verilog Model

- ▷ DARPA run users developed a model as “group ware”
- ▷ Available with permission from Tezzaron

“Assembling the reticle”

Lessons Learned

- ▷ **FORCE** everyone to use standard names for the top cell
- ▷ **Force** everyone to place origin of join metal pattern at (0,0)
- ▷ **Give EVERYONE** the top metal join layer for **EACH** of the two tiers
 - ◆ So everyone is using the same “flip” methods

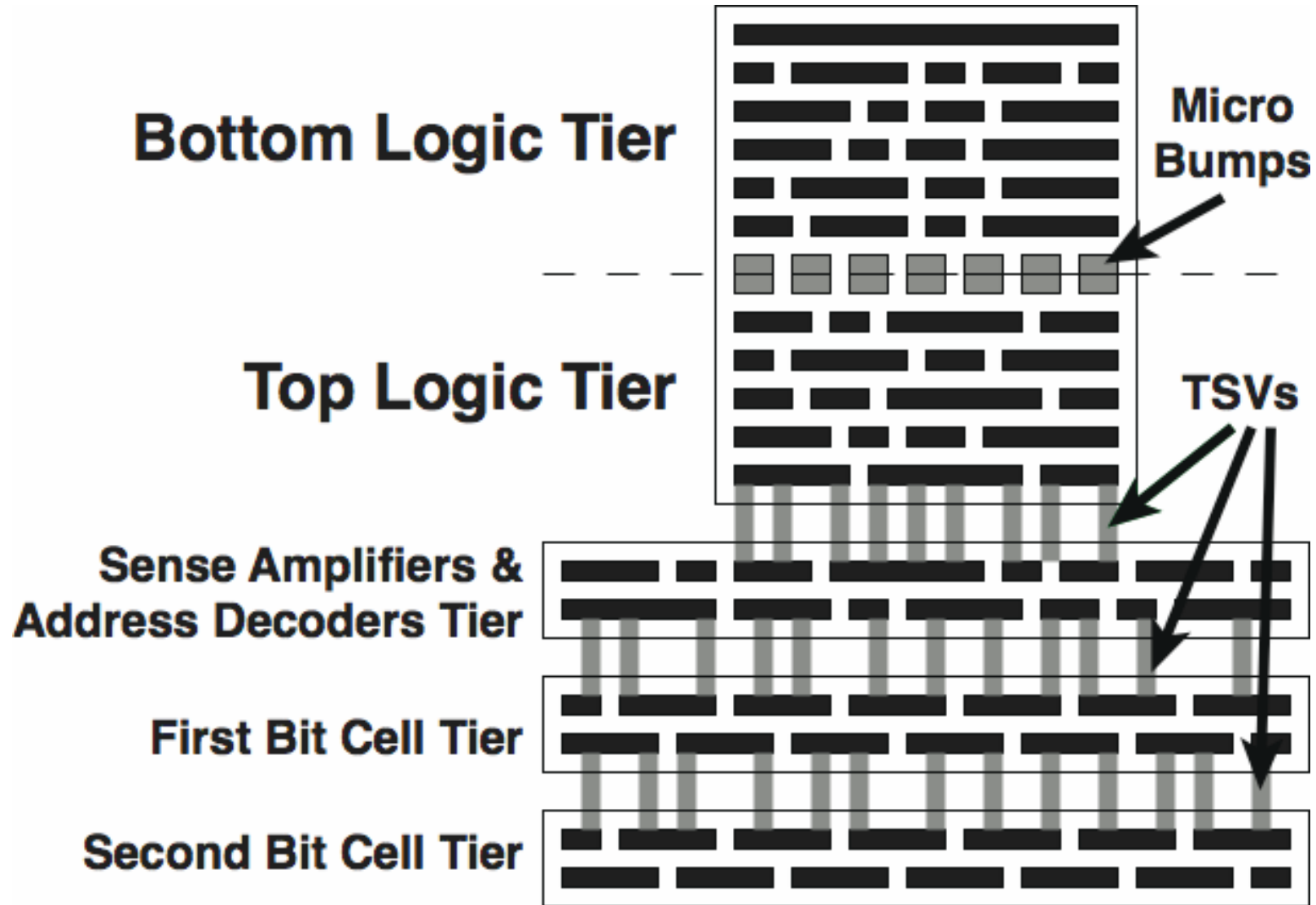
Conclusion

▷ NCSU Tezzaron Design Kit

- ◆ The TDK allows the use of the original Chartered 2D DRC and LVS decks to provide 2D DRC and full 3D LVS checking for multi-tier designs.
- ◆ 3D DRC is provided by Tezzaron's deck.
- ◆ Trivial to install on Linux, straightforward to install on other Unix variants, although SunOs could cost you an extra 10 to 15 minutes of setup time.
- ◆ Money back guarantee!

Backup Slides

Tezzaron Process



Tezzaron System Overview

