3D motivations for High Energy Physics

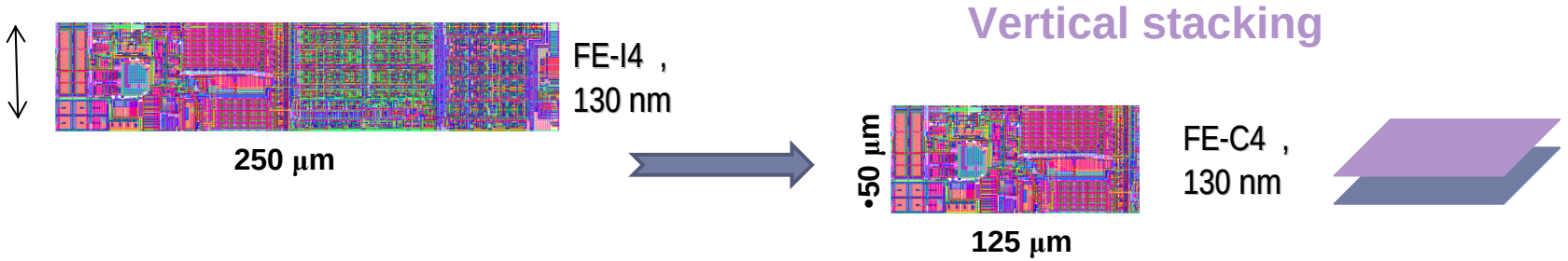
And for imaging devices

Applications of 3D IC in High Energy Physics

- Interest mainly focused on detectors with high electronic densities (Vertex detectors)
  - See Ladislav Andricek talk on this conference
  - Either Hybrid or MAPS pixels designers are interested in 3D electronics for future upgrade or new detectors
  - **Hybrids** → Decrease the pixel pitch while keeping same functions
    - Addressed at the moment by changing technology node
    - ATLAS : IBM : 0.25 µm → ATLAS Internal B-Layer upgrade : IBM 0.13 µm
    - SLHC : 90 nm or 65 nm node **or 3D**
      - Analog design challenge beyond 90 nm
      - 2 tiers of 130 nm are competitive with 1 tier of 60 nm
      - Mixing technologies will be a must
  - **MAPS** : Increase the pixels functions while keeping same pixel dimensions

Projects in hybrid pixel community in France

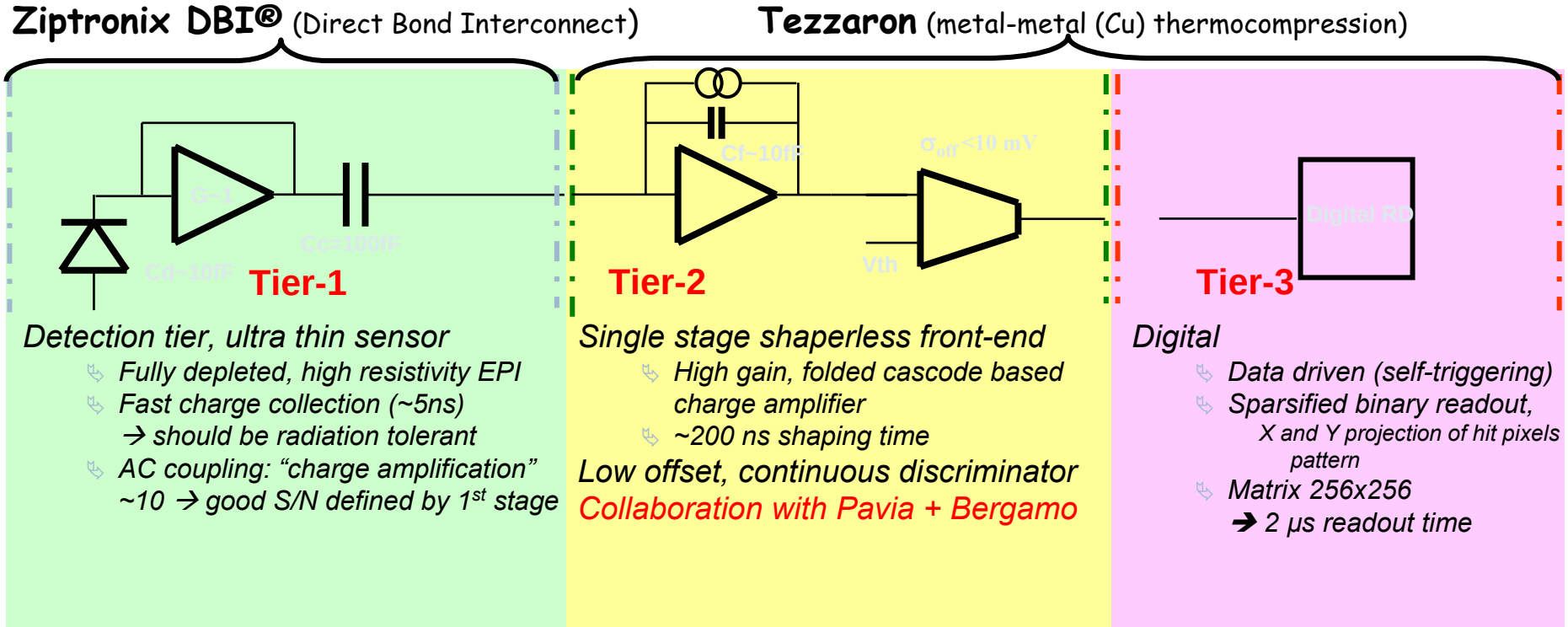
- 3D chip for SLHC or ATLAS upgrade (CPPM)
  - Split the functionalities of the “just designed” FE-I4-A , 130 nm chip into 2 tiers, having a pixel dimension of 50 * 125 µm



  - Natural separation of pixel functions
  - Quite huge chip (2*2 cm, more than 50k Pixels)
  - Common project with Bonn and LBNL groups
- New pixels concepts for achieving smaller dimensions and low power consumption
  - Reach 50*50 µm pixel pitch with 3 µW/ pixel
  - Project of LAL (Orsay) group

Projects from the MAPS community in France (IPHC/IRFU)

- Tracking and imaging : Self-Triggering Pixel Strip LikeTracker(STriPSet)



Detection tier, ultra thin sensor
- *Fully depleted, high resistivity EPI*
- *Fast charge collection (~5ns)*
  → should be radiation tolerant
- *AC coupling: "charge amplification" ~10 → good S/N defined by 1st stage*

Single stage shaperless front-end
- *High gain, folded cascode based charge amplifier*
- *~200 ns shaping time*

Low offset, continuous discriminator

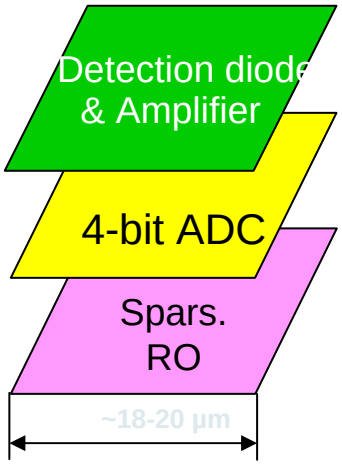
Collaboration with Pavia + Bergamo

Digital
- *Data driven (self-triggering)*
- *Sparsified binary readout,*
  X and Y projection of hit pixels pattern
- *Matrix 256x256*
  ➔ 2 µs readout time

Projects from MAPS community (con't)

- ILC /CLIC --> Fast 3D sensor with power reduction

MAPS with fast pipeline digital readout aiming to minimise power consumption (R&D in progress)



➔ σ_{sp} ~ 2 µm, $T_{int.}$ < 10 µs

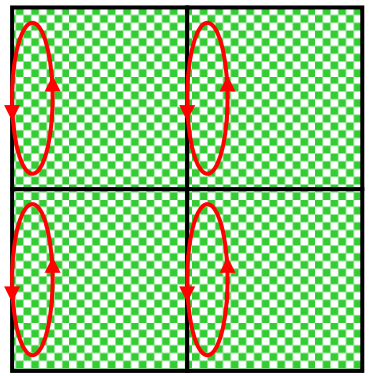
Subdivided sensitive areas running individually in rolling shutter mode

Number of rows adapted to the required readout time

- *Few µs r.o. time may be reached*

Pixel pitch ~20 µm:

- *Tier 1: CMOS sensor & preamplifier (G ~ 500 µV/e-)*
- *Tier 2: 4-bit pixel-level ADC with offset cancellation*
  - *LSB ~ Noise; ~100 µw/pixel in the selected row*
- *Tier 3: Fast pipeline readout with data sparsification*



Finally ..

- For vertex pixel detectors, 3D technologies are very promising
  - Either for right technology choice either for increase pixels functionalities
- 15 research labs joined for making the first HEP , 3D run, 2 years ago (Chartered-Tezzaron techno)
- This first experience shown that design rules and methodology are difficult to handle in such a “prototype tech”
- First results are foreseen in early 2011
- Next run (with techno variant) is foreseen in 2nd quarter of 2011 and a big part of reticle is already allocated