

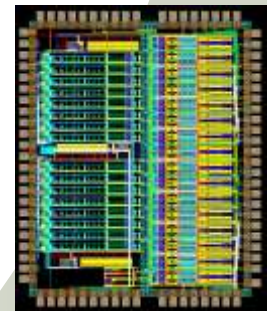
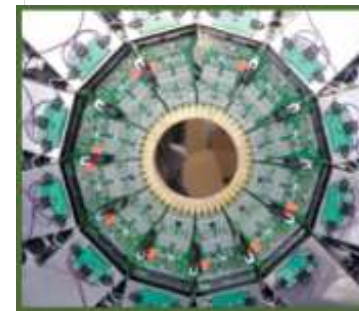
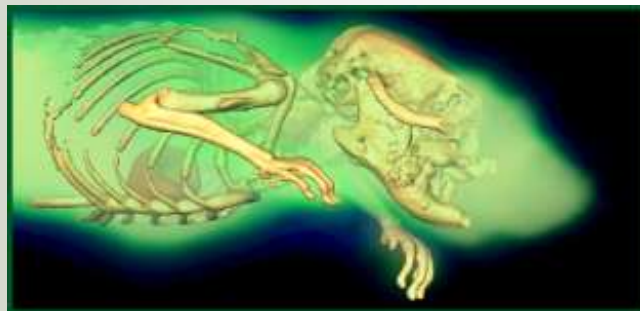
IEEE 3DIC Conference, Munich

November 18th 2010

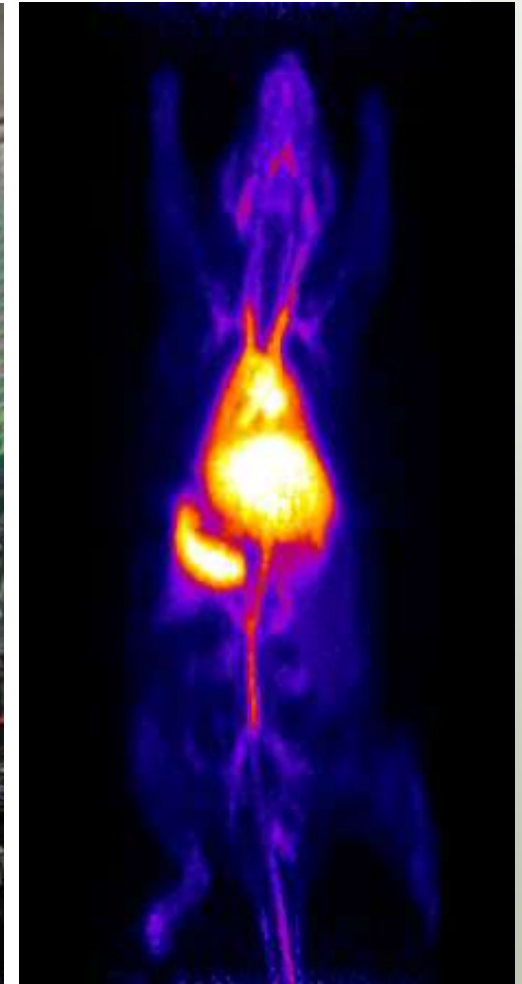
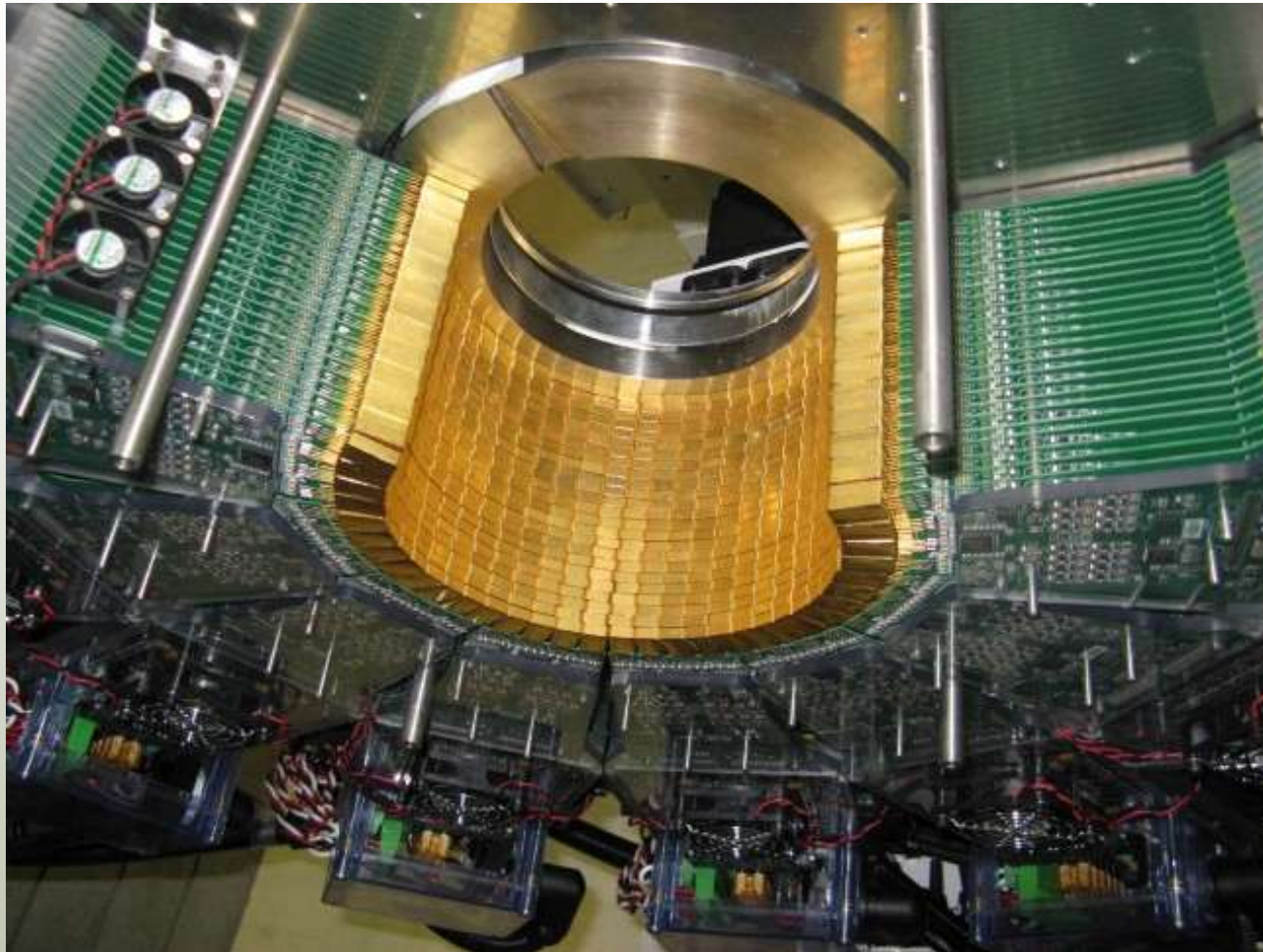
High Sensitivity Fully Digital Photodetector

Jean-François Pratte

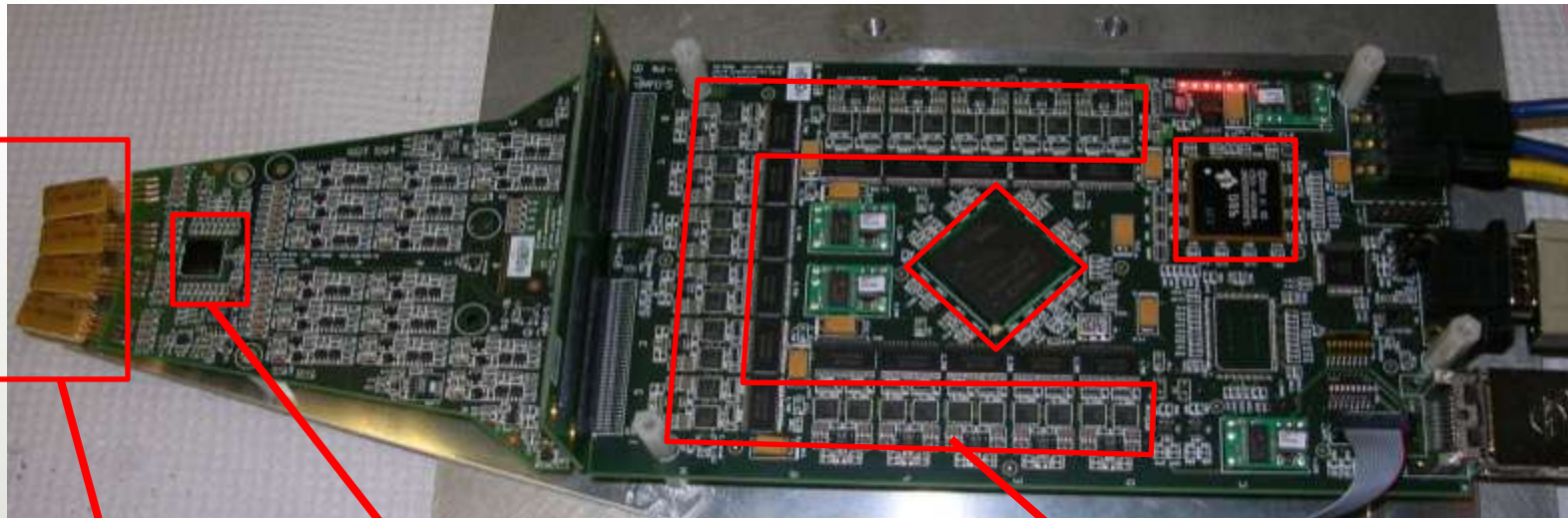
Marc-André Tétrault, Réjean Fontaine



Instrumentation for Medical Imaging



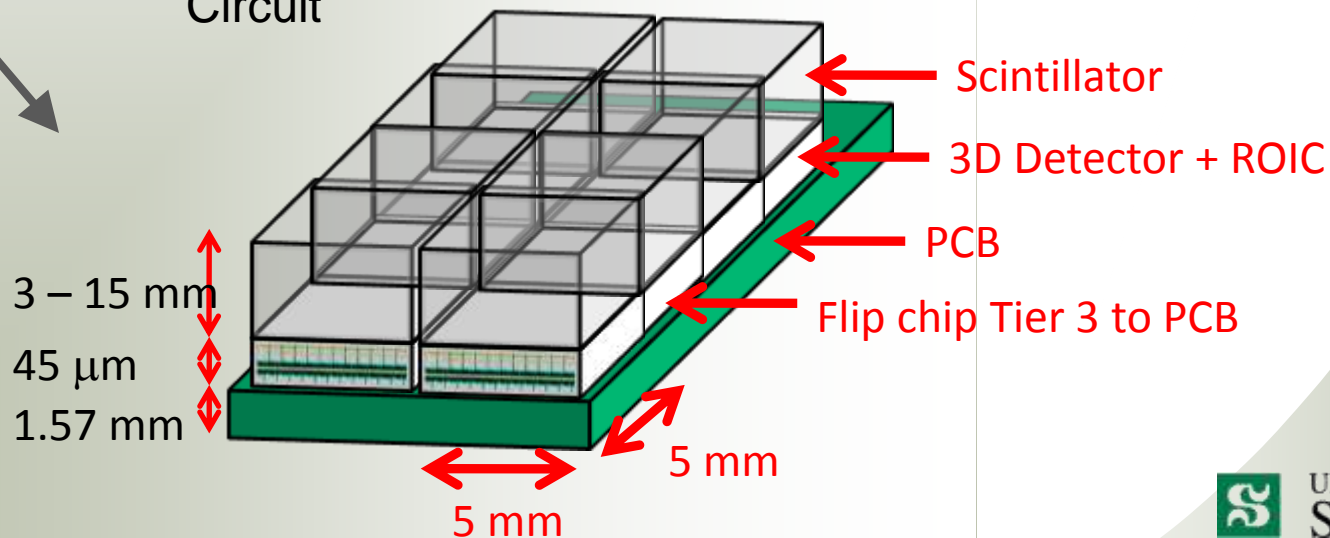
Electronic Flow



Detector

Custom Analog
Circuit

ADCs and Digital Logic



3D Stack-up

- Single photon detectors
- Tailored read-out electronic
- Application specific
 - ps Timing
 - Photon Counting
 - Interface with DAQ

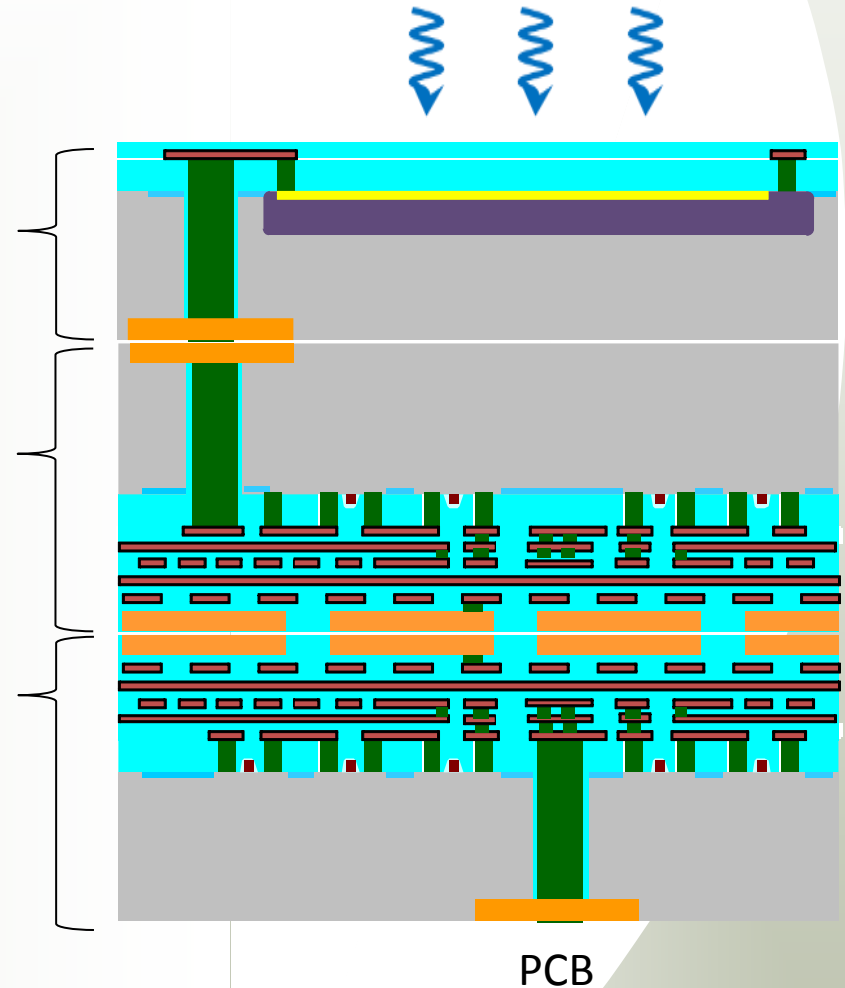


Image template: Robert Patti

Canada's National Design Network



- Creation and application of micro- and nano-system knowledge
- Supports research in Canadian universities (43)
- Diverse research areas and technologies
- Almost 400 prototyping projects per year (> 30 integrated microsystems)
- Path to commercialization of related devices, components and systems.

Supporting 3D-IC Design in Tezzaron Technology



- **CMC is partnering with MOSIS and CMP to offer MPW services based on Tezzaron technology**
 - Providing access to 3D IC fabrication (First participation in the March 2011 run)
 - Releasing Cadence-based design kit to its clients
 - Providing engineering consultation and support regarding the technology, design kit, design method and test strategy
 - Providing relevant packaging & assembly services
 - Providing access to relevant test equipment
- **CMC is de-risking use of the technology:**
 - Accelerate learning, knowledge building, design methodology development and 3D IC technology exploitation.
 - Five Canadian universities are currently designing
 - Two other Canadian universities in the process of getting access
- **CMC will continuously enhance its products & services portfolio to serve 3D IC and, more broadly, 3D integration R&D with the emphasis on heterogeneous integration.**

Progress

- Environment and **tool integration with PDK** from 3D Consortium and CMP/CMC/MOSIS
 - 2D and 3D DRC, LVS, file version management
- Lef/Def **mixed signal flow** mini-tutorial
 - Parasitic extract simulation (**hierarchical**) with digital back annotation
 - Scripts for macro placement (TSVs, BDI)
- Detailed **design** (schematics/HDL/layout), test plans

To do

- First **3D chip** run!
- High voltage TSVs (detector bias)
- High voltage (> 5 V) transistors
 - With **Chartered** process
 - Use dedicated HVCMOS tier

Acknowledgements

- Gabriella Carini (BNL)
- Grzegorz Deptuch (FNAL)
- Claude Colledani & Frédéric Morel (ICHP)
- Jean-François Boland (ETS)
- Roger Lecomte (CIMS)
- Hsu Ho (CMC)



3IT

C2MI



Faculté de génie Faculté de médecine et des sciences de la santé