3DIC Multi-Project-Wafer Program:
A Collaboration to Provide Fabrication Access

18 November, 2010

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CMP/CMC/MOSIS partner to introduce a 3DIC process MPW: Outline

- 3DIC from Tezzaron – A Commercial Foundry Process (Chartered/GF)
- The first MPW run is targeting May 2011 (other dates TBD):

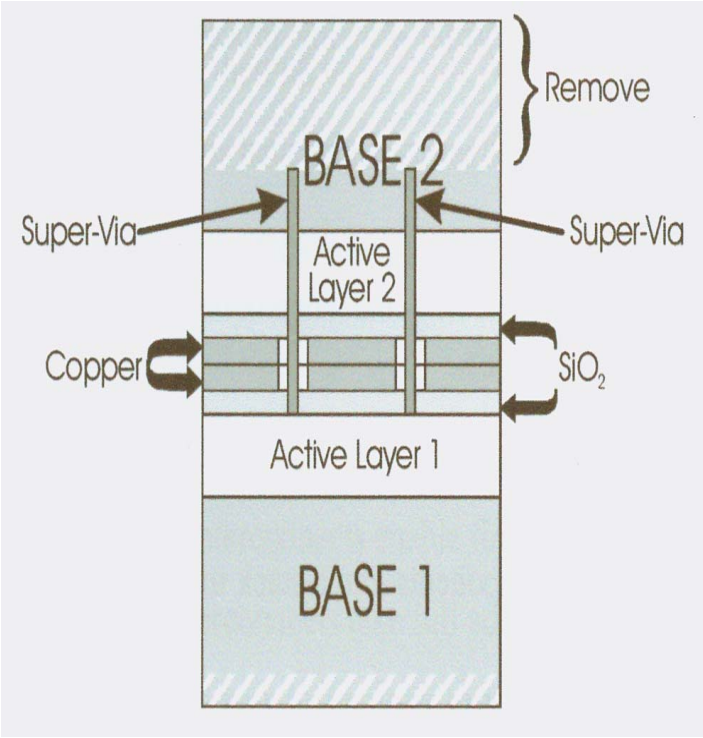
- 2-tier face-to-face bonded wafers

- 130nm CMOS process for both tiers

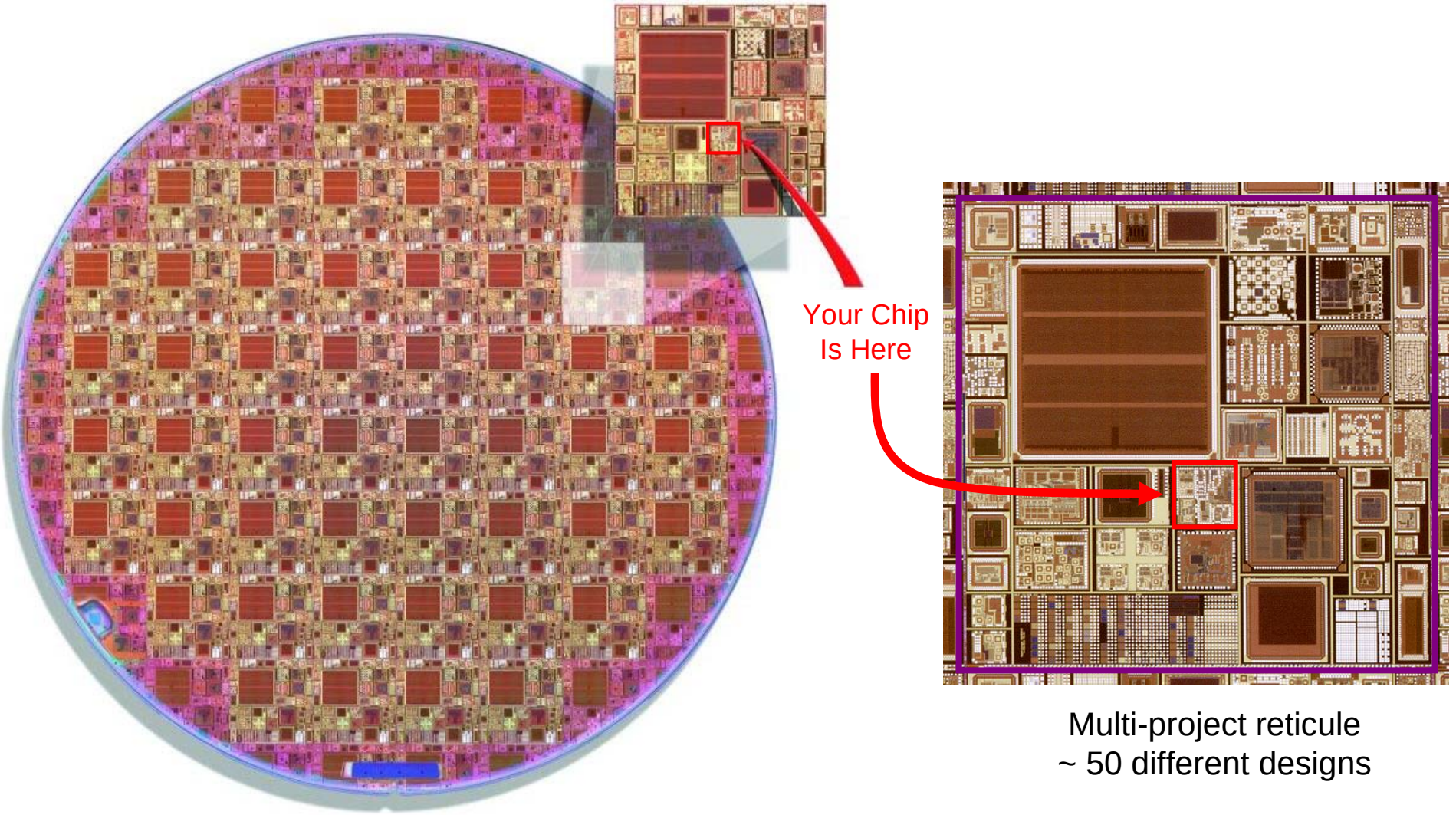
-Top tier exposing TSV and backside metal pads for wire bonding.

- A design-kit supporting 3D-IC design with standard-cells and IO libraries is available.

- Future Applications of 3DIC



MOSIS Multi-Project Wafer (MPW)



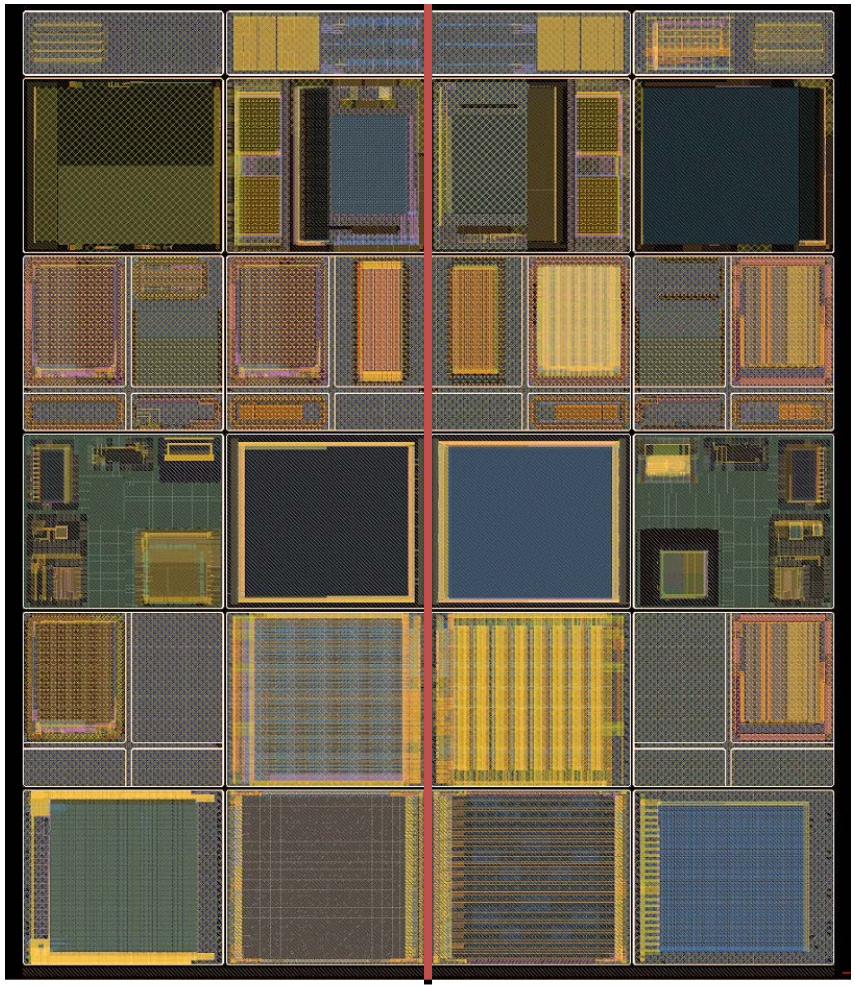
Multi-project reticule
~ 50 different designs

Shared costs: mask, wafer, and foundry and packager interface.

MPW Challenges:
Two MPW Strategies for 3DIC

- Full Reticule – Two Different Reticule Sets for a Two Tier Stack.
  - Purchase Two Reticule Sets and Two Different Wafer Lots.
  - ➢ Allows Large Chip Sizes
- Small Chips, Less Than 50% Reticule Fill.
  - Share one Reticule Set and Purchase One Wafer Lot.
  - ▪ Lower Cost Option

MPW Full Frame – Single Reticule



Subreticules:
5.5 x 6.3 mm

Notice the Mirror Image Symmetry about vertical center line

Top tiers

Bottom Tiers

This example was from FermiLab for the first High Energy Physics 3DIC Run

Tezzaron 3DIC Technology

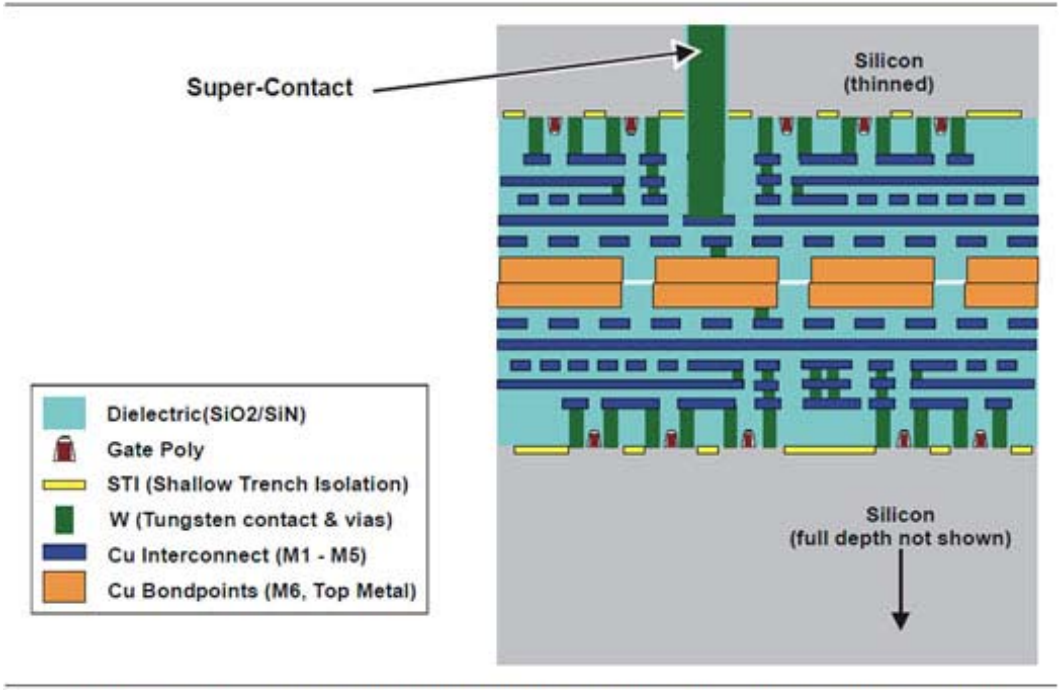


Figure 1 – Cross-section diagram of two bonded wafers after thinning

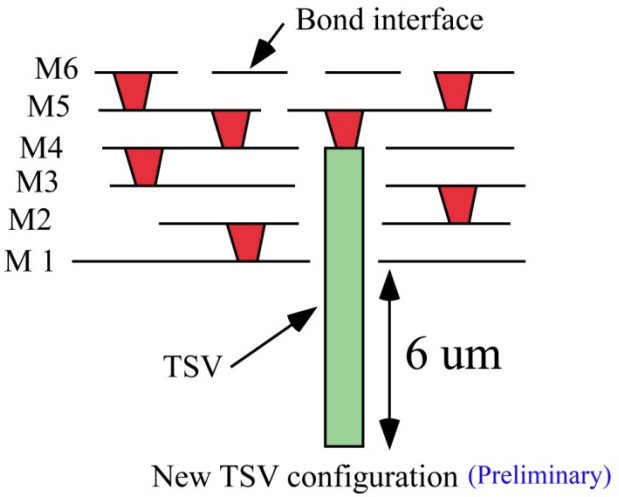
Top Si typically thinned to < 10 um

Face-to-face Cu thermo-compression bonding

Two face-to-face bonded 130 nm bulk CMOS tiers

Process Characteristics – General Flow

- GlobalFoundries 130 nm CMOS technology fabricated up to Metal 4 and Capped.
  - TSV Middle Process Strategy
  - Routing on Metal 1 to 4 is restricted to accommodate TSV's.
  - Capacitors will be VPP
- TSV's etched at SVTC along with Patterning Metal 5 and Metal 6.
  - Future: Include MiM Capacitors and 7 Metal or 8 Metal Stacks.



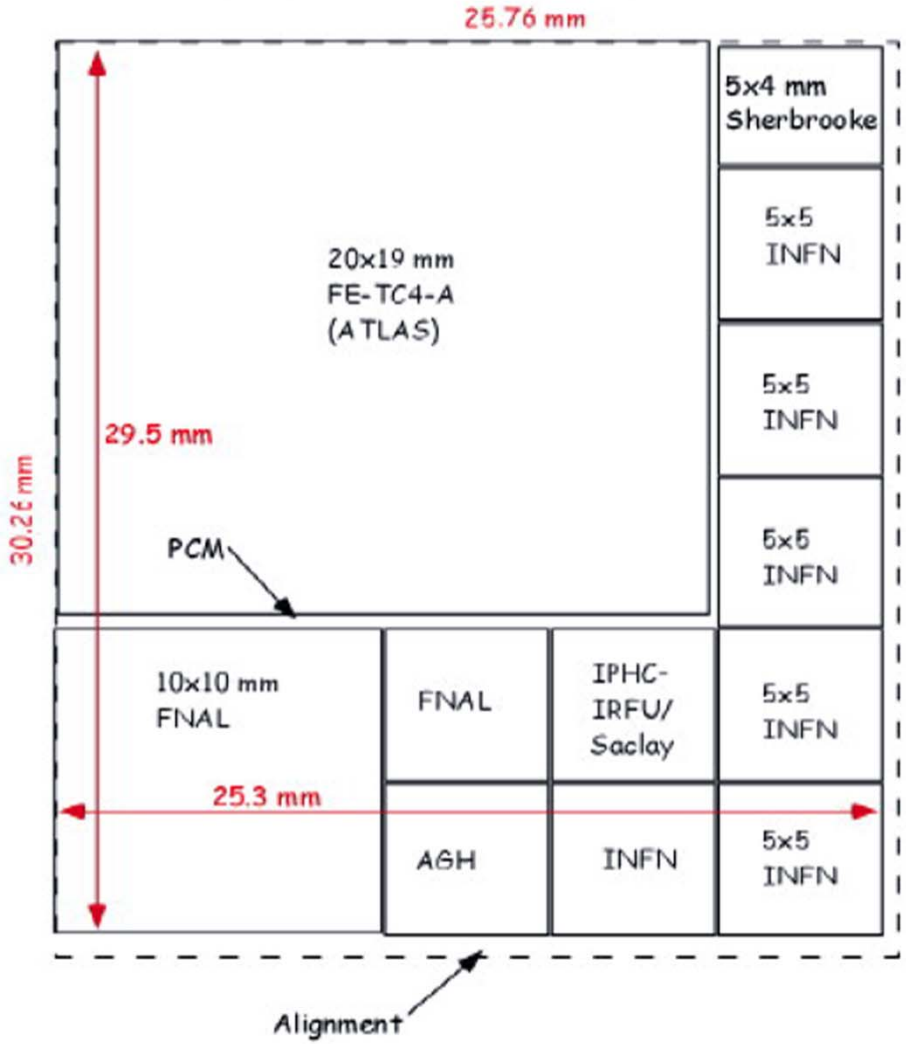
New TSV configuration (Preliminary)

Note: TSV Etch after M4 Decouples CMOS Foundries from Specialized 3DIC Processing and Therefore Enables Any CMOS Foundry for 3DIC

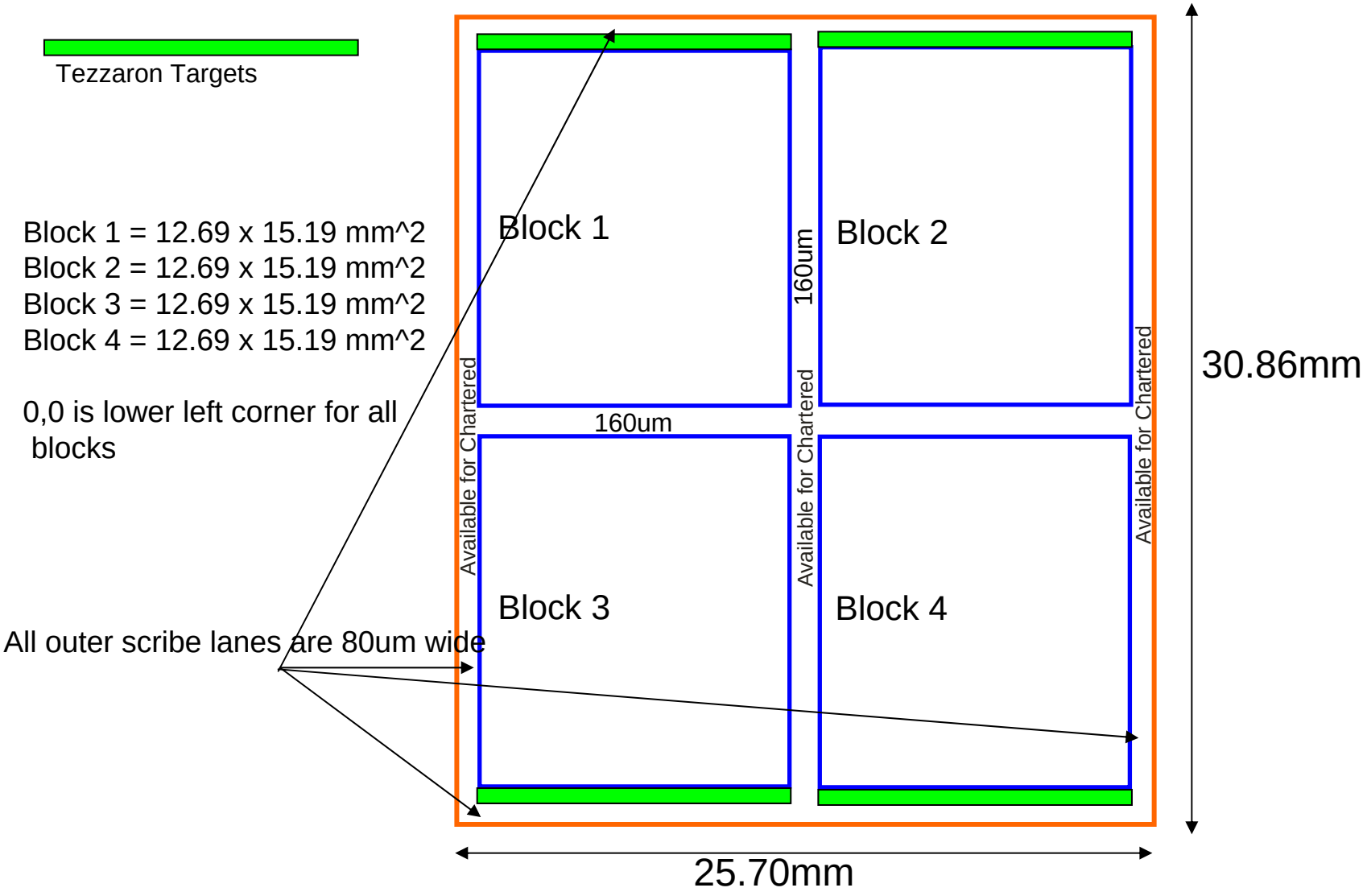
Process Options

- Transistor IO/Core options: 2.5V./1.5V. or 3.3V./1.5V. (all designs on the MPW must be the same IO/Core transistor options)
  - High voltage transistors are not available at this time.
- Transistor Thresholds: 1.5V. core circuit transistors may have standard Vt, Low Vt and Native Vt (zero Vt).
  - In the near term high Vt is not available.
- Deep N-Well
- High Resistance Polysilicon
- A capacitor is available as a VPP (Vertical Parallel Plate) Structure
- Standard metal stack will be 6 metal layers.
  - Note that the TSV etch will occur after Metal 4 which will impose metal 1, 2, 3, and 4 routing restrictions to allow for TSV etch.

Preliminary Reticule Plan – May 2011



Baseline Reticule Plan



This will be Modified as needed to serve both Customer and Foundry Requirements

Tezzaron/GlobalFoundries Design Platform

- Creating a Common root installation for the different parts of the Design Platform
  - PDK
  - Libraries
  - Memory Compilers
  - Utilities
  - Tutorials
- Defining a unique variable for the root installation. All of the modules inside refer to this unique variable.
- The Design Platform will be portable to any site without configuration scripting.
  - The user just defines the path to this variable.
- More Details on the Design Platform in the Design Tools Presentation

Future Applications of 3DIC: Mixed Technologies

- Implement a number of standard Electronic System Platforms to support research in new technologies: The Silicon Workbench
  - Creates analog and digital test systems for research:
    - Photonics
    - Graphene / Carbon Nano-Tubes (CNT)
    - MEMS

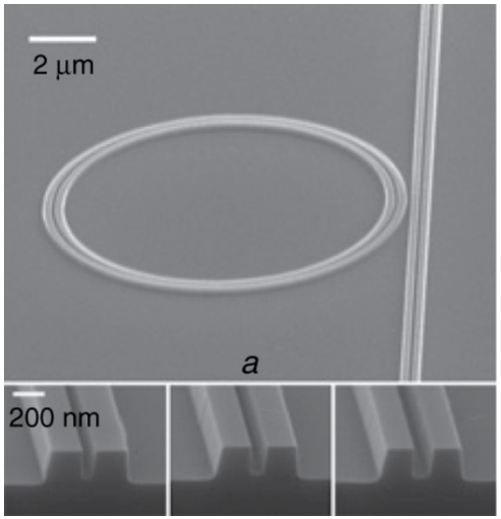
Silicon Workbench

- 3DIC Silicon Workbench Serves as an Electronic Control System Interface to Other Technologies
  - Permits Separation of Non-Silicon Technologies from the Constraints of Commercial CMOS.

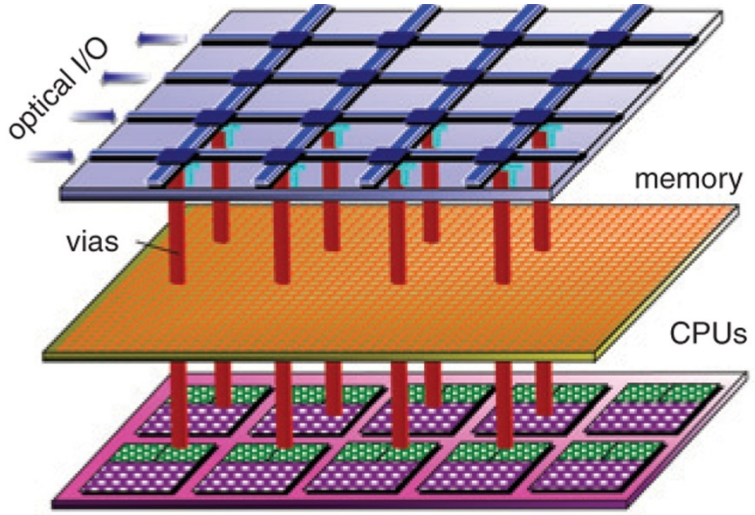
- Production of Commercial Mixed Technology 3DIC is Commercially Viable.
  - Brokered 3DIC MPW Exists Now using Tezzaron-GlobalFoundries for 3DIC (MOSIS, CMP, CMC)

Silicon Workbench for Photonics

Electronic – Photonic Integrated Circuit (EPIC) :



CMOS-Compatible Ring Resonator *

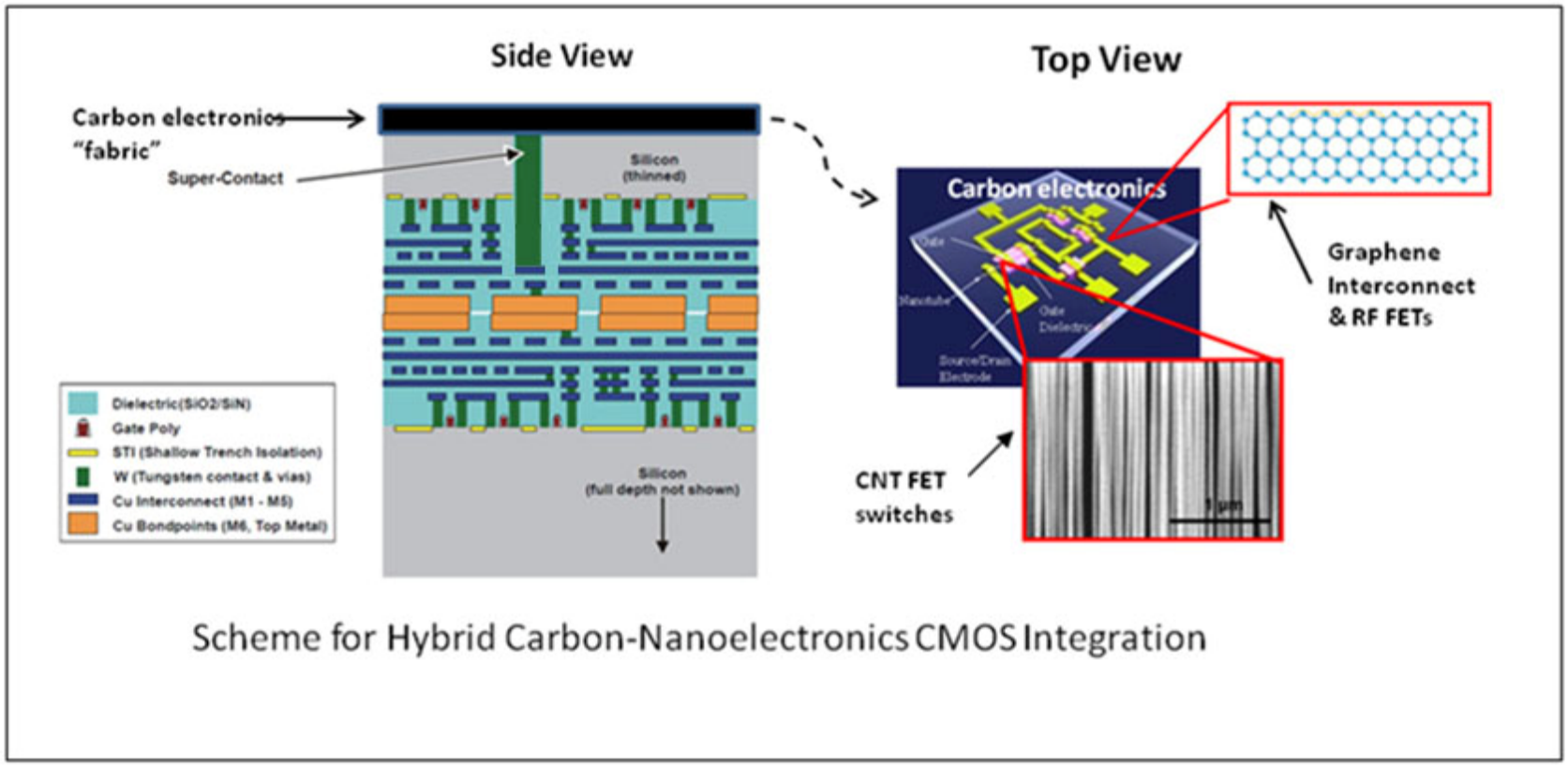


EPIC in a 3DIC Structure *

- EPIC using both CMOS and 3-Dimensional Integrated Circuit Techniques (3DIC)
- Ring Resonators Support Wavelength Dependent Signal Routing
- Other Photonics Technologies may be used such as Indium Phosphide

* Yoo, S.J.B. – "Future Prospects of Silicon Photonics in the Next Generation Communications and Computing Systems", Electronic Letters, Vol. 45, No. 12, 4 June, 2009

Leveraging 3DIC MPW Run for Carbon Electronics Interfaced to Commercial CMOS



Scheme for Hybrid Carbon-Nanoelectronics CMOS Integration

Silicon Workbench for MEMS and III-V Compound Semiconductors

- III-V Compound Semiconductors stacked on top of a silicon workbench adds technology diversity to systems on a single footprint.
  - Avoids technology incompatibility
- MEMS structures are not constrained by CMOS technology fabrication processes.
- Support Graphene / Carbon Nanotube Research.
- New innovative systems become practical.

What is the Next Step?

- Creativity – Innovative collaborations with mixtures of technologies will lead to radically improved systems.