



Announcement

65nm PDK for Tanner Tools available from CMP

Grenoble, FRANCE, December 3rd, 2010, CMP (Circuits Multi Projets[®]) announce it has released the Tanner[®] Process Design-Kit (PDK) for the 65nm CMOS process it offers.

The PDK allows both front-end and backend designs covering all the features offered in the Tanner Tools Pro[®] package.

Schematic capture is available with S-Edit[®], electrical simulation available with TSpice[®], layout generation using L-Edit[®], and DRC LVS verifications. All have been customized with the 65nm design-rules and electrical parameters.

The basic devices have been implemented in the PDK, allowing mixed signal A/D design.

MOS devices are available, standard/high/low VT for both the General Purpose (GP) process flavor as well as the Low Power (LP) process flavor.

Resistors and capacitors have been also included for simulation, layout, and DRC / LVS.

The next PDK release will fully support the HiPer[®] Design Suite from Tanner.

The PDK is available under NDA, for free from CMP.

Contact: cmp@imag.fr

On-Line Request: <http://cmp.imag.fr/products/DK/dkrequest.php>

About CMP

CMP is a service organization in ICs and MEMS for prototyping and low volume production. Circuits are fabricated for Universities, Research Laboratories and Industrial Companies. Advanced industrial technologies are available in CMOS, BiCmos, SiGe BiCMOS and MEMS etc. CMP distributes and supports several CAD software tools for both Industrial Companies and Universities. Since 1981, more than 1000 institutions from 70 countries have been served, more than 6000 projects have been prototyped through 700 runs, and 56 different technologies have been interfaced.

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