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STMicroelectronics and CMP to offer CMOS processes to Chinese universities

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Key elements of the initiative are that STMicroelectronics (ST) will ensure the certification of the local partners and the fabrication of the ICs designed by the universities, while CMP will be the interface for commercial and technical aspects, from the distribution and support of the CAD software tools and design kits, up to the delivery of the samples. This mechanism will allow Chinese research organizations to obtain small quantities of advanced ICs. The availability of real silicon will enable them to validate design ideas. The ST process technologies available via CMP include 120nm, 90nm and 65nm CMOS technologies, with multiple transistor flavors from ultra-low leakage to high-speed and complete standard cells and I/Os libraries. Laurent Perier, director of China IC Design Centers for STMicroelectronics, said: "Ensuring that Chinese universities have access to our technologies is testimony of our commitment to work with Chinese partners in their path towards innovation."