II - INTEGRATED CIRCUITS MANUFACTURING

A - Main data

Main data concerning the circuits fabricated in 2010 are the following:

- 354 circuits for Research (210), Education (43) and Industry (101)
- 11 technologies in CMOS, BiCMOS, SiGe BiCMOS, and MEMS
- 108articipating Institutions from 23 countries
- 101 circuits fabricated for industrial purposes for 25 Institutions in prototyping or low volume
- 27 MEMS circuits were fabricated in MUMPS technologies and CMOS bulk micromachining

B - Circuits' list and processing for each run

B.1 - Run tables in 2010

austriamicrosystems 0.35 µm CMOS

A35C10_1
Technology: austriamicrosystems 0.35 µm CMOS C35B4C3
Starting date: 05 February 2010
Delivery of chips: 07 May 2010

Institution	Town	Country	Top Cell	E R I	Function
Federal University of Rio de Janeiro	Rio de Janeiro	BR	imager01	R	This is IC performs a focal plane image compression of an image of 32x32 pixels.
CMC/Queen's University	Kingston	CA	ICMPMPRD	R	Filterless CMOS image sensor, with single slope ADC with adaptive quantification steps.
LETI/CEA	Grenoble	FR	TOP_CINESIC_8V	R	
LETI/CEA	Grenoble	FR	VHDR_FE1	R	RFID card circuit for high data rates (up to 5.1Mb/s)communications at 13.56MHz carrier. The circuit is also a high power supply provider. Corrected version of the OMAPV4.
Observatoire Meudon	Meudon	FR	YHasicN5	R	Proximity electronics for a flight camera based on an IR or visible matrix detector.
Observatoire Meudon	Meudon	FR	YHasicN6	R	Proximity electronics for a flight camera based on an IR or visible matrix detector.
Ecole Polytechnique	Saint Maur des Fossés	FR	detec16ch	R	LPP has a well know ability to design and build instrumentation for space plasmas investigations. Since a few decades we have been developping C magnetometers and particule detectors which have been flownonboard many international spacecraft. This ASIC is a new technological step of the electronical devices which we designed 16 chanels of charge amplifier and discriminator for Micro Chanel Plate.
INSA Lyon	Villeurbanne	FR	FC0210	R	Transistors, capacitor and inductor test structures.
Hong Kong U. of Sc. & Techno	Kowloon	HK	SIMO_LDO_DESIGN	ER	An single input inductor multipel output boost mode power converter and Low Dropout Regulators for academic research.
Hong Kong U. of Sc. & Techno	Kowloon	HK	SIMO_LDO_DESIGN_2	ER	A single input single inductor multipel output buck mode power converter and Low Dropout Regulators for academic research.
Hong Kong U. of Sc. & Techno	Kowloon	HK	top_A35C10_1_V1	R	Image sensor (CMOS) for research purpose.
Chinese U. of Hong Kong	Shatin	HK	SMPC_TOP_X5	E	Switching mode mulltiple channel buck-boost converter.
INFN-Bari	Bari	IT	Gastone64_v2	R	Gastone chip for Kloe Inner tracker readout.
Politecnico di Bari	Bari	IT	ADC_test	R	The circuit contains an 8-bit-two-step, interlead, flash ADC to be integrated in a future version of a front-end chip for silicon Photo-Multiplier detectors. Also a standalone analog front-end channel and a current reference circuit have been integrated for testing purposes.
Politecnico di Bari	Bari	IT	basic32_new	R	
Tokyo University of Science	Tokyo	JP	KIYOCHIP	R	Image sensor.
National Univ. of Singapore	Singapore	SG	wholechip	R	This is an UWB transceiver.
Mikroelektronik Arastirma Gelistirme Tasarim ve Ticaret Limited Sirketi	Istanbul	TR	OEALDO_1p0_wPAD	I	The IC is a Low Dropout Regulator.
University of Southampton	Southampton	UK	prw_feb_2010	E	Mixed signal IC with AD converters.
University of Southampton	Southampton	UK	razorchip_2	E	Mixed signal IC with AD converters.
14 Institution(s)			**20 Circuit(s)**		

A35C10_2
Technology: austriamicrosystems 0.35 µm CMOS C35B4C3
Starting date: 21 May 2010
Delivery of chips: 31 August 2010

Institution	Town	Country	Top Cell	E R I	Function
Univ Federal Santa Catarina	Florianopolis	BR	LCImai10	E	There are five projects in this IC: - A class-D amplifier for hearing aids devices. This is a front-end amplifier designed in current mode for low power, low voltage operation. - A NMOS specific current generator with ultra-low power consumption. - A PMOS specific current generator with ultra-low power consumption. - Test structures for stress measurements. The objective of theses structures is the study of the aging effect and the hot carrier injection in different types of geometrical transistor. - Low noise amplifier for hearing aids devices. This is a back-end amplifier designed in current mode for low power, low voltage operation.
Univ. Federal Santa Maria	Santa Maria	BR	layout_chip2	E	This circuit is an operational amplifiers with reconfigurable input differential pair, using series-parallel association of transistors, reconfigurable by external pins and internal registers. This aims minimum points searching on offset and noise or maximum points search on common mode and power supply rejection ratio. The reconfiguration aims compensate mismatches on fabrication. Also, in the same die, there is an ultra-low power successive approximation register analog to digital converter, and a ultra-high speed ADC for ultrawide band systems.
CMP	Grenoble	FR	top_PV_run2	R	
LPSC/IN2P3	Grenoble	FR	full_Chip	R	Low power analog to digital converter.
Faculté des Sciences de Limoges	Limoges	FR	CPLG_2_25_Xlim	R	
Faculté des Sciences de Limoges	Limoges	FR	XRAD_XLIM_V1	R	
Observatoire de Paris	Nançay	FR	ELISA_03_HF	R	
InEss	Strasbourg	FR	IRMXYZ02	R	The circuit is intended for magnetic field measurement in MRI environment. It features Hall effect devices with biasing and signal conditionning circuits.
Hong Kong U. of Sc. & Techno	Kowloon	HK	Bp_detector	ER	The circuit is an analog front-end detector for micro-electrode array (MEA) detection with the purpose of academic publication Now MEA is commonly used to record extra-cellular bio-potentials for varieties cell studies. The circuit on chip includes the front-end analog processing circuit and a SAR-ADC.
Centre for Development of Advanced Computing	Kerala	IN	HDG035D	R	A data convertor circuit and various submodules which contains comparators, transconductance amplifier and digital filter.
NARA Inst. Sc. & Techno	Nara	JP	CA35C102AT_4w_mim	E	Small image sensor for Bio imaging.
NARA Inst. Sc. & Techno	Nara	JP	CA35C102KS_CDS	E	Image sensor TEG.
Korea Advanced Institute of Science and Technology	Daejon	KR	KAIST	R	Biosensor for single cell impedance.
Linköping University - ISY	Linköping	SE	Chip1_Final_Topcell	E	2 projects for education : A DDL and a digital transceiver.
Linköping University - ISY	Linköping	SE	Chip2_Final_Topcell	E	4 projects for education : Two high speed DACs and two Successive Approximation ADCs.
Linköping University - ISY	Linköping	SE	Chip3_Final_Topcell	E	4 projects for education : Two FM transmitters and two BFSK Modulators.
Linköping University - ISY	Linköping	SE	Chip4_Final_Topcell	E	3 projects for education : Two Sigma-Delta Modulator ADCs and one Successive Approximation ADC.
Linköping University - ISY	Linköping	SE	Chip5_Final_Topcell	E	2 projects for education : Two Signal-Delta ADCs.
Linköping University - ISY	Linköping	SE	Chip6_Final_Topcell	E	2 projects for education : Two hign-speed digital transceivers.
Nanyang Technolo. Univ.	Singapore	SG	ADC12_10_final5	ER	This is analog-to-digital converter.
Nanyang Technolo. Univ.	Singapore	SG	AUDIOB_3CHL2_TRX	R	Low power OOK transceiver
National Univ. of Singapore	Singapore	SG	BMDA_chip	R	This is a signal read-out front-end designed for biomedical data acquisition.
National Univ. of Singapore	Singapore	SG	TOPCHIP_NUSMPW2105	E	High performance Biomedical testchip.
Iowa State University	Ames	US	SPBUCK	R	600mA, 5V to 1.8V Step-Down switching power converter using Spread-Spectrum control technique for switching noise manipulation. In target application is mixed-signal Systems-On-Chip with extensive analog/RF content.

MOSIS	Marina del Rey	US	V05MAA	R	The circuit is designed to execute a neural signal processing algorithm for real-time rejection of stimulus artifacts in recorded neural data.
University of Texas at Dallas	Richardson	US	convt	E	DC-DC converter. The aquired items will be used to verify the designed circuit performance for academic research paper.
University of Texas at Dallas	Richardson	US	sub_MIM021vs	E	The aquired items will be used to verify the designed circuit performance for academic research paper.
17 Institution(s)			**27 Circuit(s)**		

A35C10_3
Technology: austriamicrosystems 0.35 µm CMOS C35B4C3
Starting date: 09 July 2010
Delivery of chips: 15 October 2010

Institution	Town	Country	Top Cell	E R I	Function
Universidade de Brasília-Faculdade de Tecnologia	Brasilia	BR	UNB0710	ER	The design sent for prototyping consists in some circuit blocks that will be used to validate some design methodologies adopted by our research team. These blocks consist on a LNA amplifier, VCos, an operational amplifier, an signal conditioner, a digital interface, and isolated subcircuits.
Balearics Islands University	Palma de Mallorca	ES	radsens	R	Sensors for gamma radiation and magnetic field.
CMP	Grenoble	FR	TOP_COMMUN	R	
LPSC/IN2P3	Grenoble	FR	osc16_top	I	Sinus generator array for microfluidic microsystem control; for biomedicals cells separation.
LETI/CEA	Grenoble	FR	TOP_BMS_TEST	R	
LIRMM	Montpellier	FR	BOBST_V1	R	Test bench for SRAM memories.
InEss	Strasbourg	FR	IRMXYZ03	R	This circuit is intended for magnetic field measurement in MRI environment. It features Hall effect devices with biasing and signal conditionning circuits.
IMS	Talence	FR	ASICMinimum	R	Medical interface for NeUronal Stimulation (MINUS) is dedicated to acquisition of low-amplitude neuronal signals, and adaptated stimulation. The device includes different amplifiers and filters for test and characterization.
ENSEEIHT	Toulouse	FR	ASIC	R	this ASIC has been developped in AIME Toulouse by the CESR-CNRS laboratory and the INPT-ENSEEIHT-LOSE. It is composed of a 16-channels mixed-signal instrumentation chain for MicroChannel Plates. MCP are used in astrophysics to detect electrons. Each chain is composed of a charge pre-amplifier, a shaper circuit and a discriminator. A test chain with follower circuits placed at each intermediate output has been implemented too.
Hong Kong U. of Sc. & Techno	Kowloon	HK	HYS_CNVERTER_Tapeout	ER	Hys Converter.
University of Nottingham	Nottingham	UK	IFcam_Top	R	80x80 pixel camera for scientific imaging.
University of Texas at Dallas	Richardson	US	Chip1	R	The acquired items will be used to verify the designed circuit performance for research paper.
12 Institution(s)			**12 Circuit(s)**		

A35C10_4
Technology: austriamicrosystems 0.35 µm CMOS C35B4C3
Starting date: 27 August 2010
Delivery of chips: 16 November 2010

Institution	Town	Country	Top Cell	E R I	Function
Federal University of Mato Grosso do Sul	Mato Grosso do Sul	BR	MLV_ADC4BIT	R	
Federal University of Rio de Janeiro	Rio de Janeiro	BR	Filters2010	R	
CMC/Queen's University	Kingston	CA	Eyechip2	R	The project contains two parts : - The first part is a design of a CMOS image sensor 102x136 pixels for biomedical application. - The second part consists of a C MOS image sensor with high dynamic range pixel and eye adapted, Delta Reset Sampling and Current Comparators circuits.
University of Macau	Macau SAR	CN	BIORFE	R	A readout analog front-end for biopotential signel acquisition. It consists and instrumentation amplifier, a programmable-gain amplifier, and a digital filter for testing.

Universidad Autonoma de Barcelona	Barcelona	ES	NEMESYS_v3	R	Design of microelectromechanical structures (MEMS) with CMOS circuits intended for characterization. Design of Microelectromechanical structures (MEMS) with CMOS circuits intended for characterization
LPSC/IN2P3	Grenoble	FR	SAR14_v2	R	
TIMA	Grenoble	FR	imagyne4	R	CMOS Vision sensors (128x128 pixels) with a embedded ight adaptive system. CMOS Vision sensors (128 x 128 pixels) with an embedded light adaptative system
LPNHE/IN2P3	Paris	FR	PD_ULCA	R	Ultra low current amplifier for photodiode readout.
IneSS	Strasbourg	FR	CFPSOC	R	The circuit is intended for magnetic field measurement. It features a Hall effect device with its biasing and signal conditionning circuit. The circuit features also a sigma-delta modulator for signal digital conversion.
Iness	Strasbourg	FR	THERMIDEAS	R	The circuit is designed to study the thermal behaviour of integrated circuits.
IPHC-Univ. Louis Pasteur	Strasbourg	FR	AlphaRad2_Chip	R	Monolithic Active Pixel Sensor dedicated to particle detection.
Hong Kong U. of Sc. & Techno	Kowloon	HK	ZHANLU	ER	Power management IC for academic research.
Chinese University of Hong Kong	Shatin	HK	CUASIC	E	
Politecnico di Bari	Bari	IT	basic32_adc	R	This circuit is a new version of a previous front end for Silicon Photo-Multiplier detectors. The chip contains 32 analog front-end channels, each formed by an input current buffer with very low input resistance, a fast current discriminator, a charge sensitive preamplifier to integrate the current delivered by the detector, a baseline holder and a peak detector. A digital part is used for the read-out of the channels and to implement data communication with the external world. A 8-bit, two step ADC is also integrated on-chip.
NARA Inst. Sc. & Techno	Nara	JP	Ca35c104HK	E	Image sensor with electrode for bioscientific application traials.
NARA Inst. Sc. & Techno	Nara	JP	CA35C104HMKS_daisy	E	Small image sensor for Bio imaging.
NARA Inst. Sc. & Techno	Nara	JP	CA35C104TITK	E	Image sensor for artificial retina.
NARA Inst. Sc. & Techno	Nara	JP	CA35C104YS	ER	Image sensor with electrode for bioscientific application traials.
University College London	London	UK	12bitadc_test	E	Analog to digital converter.
Obsidian Technology	Dana Point	US	top	I	Test chip for PLL, Pipeline ADC, and LDO cells.
16 Institution(s)			**20 Circuit(s)**		

A35C10_5

Technology: austriamicrosystems 0.35 µm CMOS C35B4C3
Starting date: 03 December 2010
Delivery of chips: 21 February 2011

Institution	Town	Country	Top Cell	E R I	Function
Federal University of Mato Grosso do Sul	Mato Grosso do Sul	BR	MVL_GATES	R	
Ecole Polytechnique de Montreal	Montreal	CA	AMSPROTOE	R	This project aims at the design, fabrication and test of a1/4 VGA active pixel sensor array. This prototype focuses mainly on the analog aspect of the pixel circuit and the column amplifier, however, digital circuits will be use in the periphery of the array of pixels in order to perform sequential pixel reset and read.
University of Macau	Macau SAR	CN	BME_testchip_2nd	R	This chip includes three parts. The first part is a nano-watt class low pass filter for biopotential signal processing. The second part is an ECG QRS complex detection digital circuit. The third part is a multistage amplifier for driving very large capacitive loads.
Universidade Politecnica de Valencia	Valencia	ES	TOP_VIEW	R	Analog front-end for photomultiplier based gamma-ray detectors.
University of Oulu	Oulu	FI	TDC_TOP	R	Time-to-digital Converter.
Institut FEMTO-ST	Besançon	FR	merodas_v1	R	DAS measurement.
CMP	Grenoble	FR	TOP_PV_C35_8		
TIMA	Grenoble	FR	CMOS_MEMS_03122010	R	Test of MEMS structures fabricated with a sacrificial etching of oxyde layers. The structures are expected to be used in the design of acoustic sensors.
LETI/CEA	Grenoble	FR	smartcis	R	This chip is a CMOS image sensor with integrated analog image processing. A 110x240 3T pixel array with 10µm pixel pitch ais associated to a programmable switched capacitors unit and ARAM array, allowing some

					low level processing tasks. Dedicated to videosurveillance applications with strong power consumption constraints , this CMOS image sensor is able to wake up on events and track them, by applying high resolution on moving areas, while keeping background in low resolution.
L2MP POLYTECH Marseille	Marseille	FR	CAP_CQFP64_TOP	R	The circuit is an acquisition chain followed by an analog to digit conversion for electromechanical sensors.
LAL/Université Paris Sud	Orsay	FR	M2_SECI_Folded_Cascodes	E	This circuit features Folded Cascode OTAs designed by students to constitute a read-out circuit for a MEMS accelerometer.
LAL/Université Paris Sud	Orsay	FR	PACS_FPA_Macropixels_v1	R	This circuit features an electronic retina prototype for low power analog image preprocessing within a left-behing video surveillance system. Several test circuits for some of the elements have also been included.
Ecole Polytechnique	Saint Maur des Fossés	FR	dtec16chV2	R	LPP has a well known ability to design and build instrumentation for space plasmas investigations. Since a few decades we have been developping particule detectors which have been flown onboard many international spacecraft. This ASIC is a new technological step of the electronical devices which we designed 16 chanels of charge amplifier and discriminator for Micro Chanel Plate.
IneSS	Strasbourg	FR	ECG_HALL_2	R	The circuit is intended for ECG and magnetic field measurement with Hall effect devices.
IMS	Talence	FR	CALOR	ER	RFID TAG with integrated temperature sensor.
Université Paris 13	Villetaneuse	FR	Circuit2010	R	
Université Paris 13	Villetaneuse	FR	Circuit2010bis	R	
NARA Inst. Sc. & Techno	Nara	JP	CA35C105_KA_VCO	E	Voltage controlled oscillator and image sensor for bioimaging.
University of Southampton	Southampton	UK	d2_top_level_1011	E	Multiple Site Design ASIC for Microelectronics Teaching.
University College London	London	UK	BUFFERS	E	
Iowa State University	Ames	US	REGULATOR	R	600mA, 5V to 1.8V Step-Down switching power converter using Spread-Spectrum control techniques for switching noise manipulation. In target application is mixed-signal Systems-on-Chip with extensive analog/RF content.
MOSIS	Marina del Rey	US	V0BJAA	R	Photo signal detection and electric signal output.
MOSIS	Marina del Rey	US	V0BKAA	R	The circuit has amplifiers and oscillators to wirelessly transmit biopotentials.
20 Institution(s)			**23 Circuit(s)**		

SA35C10_1
Technology: austriamicrosystems 0.35 µm CMOS C35B4C3
Starting date: 03 May 2010
Delivery of chips: 12 July 2010

Institution	Town	Country	Top Cell	E R I	Function
CEA-SACLAY	Gif sur Yvette	FR	ACTA3	I	
CEA-SACLAY	Gif sur Yvette	FR	AGETV1	I	
CEA-SACLAY	Gif sur Yvette	FR	IDeFX_BD	I	
CEA-SACLAY	Gif sur Yvette	FR	NECTARO	I	
CEA-SACLAY	Gif sur Yvette	FR	PROTECT_IO	I	
CEA-SACLAY	Gif sur Yvette	FR	SAMLONG_A	I	
IPHC-Univ. Louis Pasteur	Strasbourg	FR	IMOTEPAD_V3	I	
IPHC-Univ. Louis Pasteur	Strasbourg	FR	IMOTEPAD2010	I	
IPHC-Univ. Louis Pasteur	Strasbourg	FR	M22HRes_1_FILL	I	
IPHC-Univ. Louis Pasteur	Strasbourg	FR	PETADC_top_FILL	I	
IPHC-Univ. Louis Pasteur	Strasbourg	FR	PETROC_TOP_FILL	I	
IPHC-Univ. Louis Pasteur	Strasbourg	FR	Top_latchUp_HR	I	
IPHC-Univ. Louis Pasteur	Strasbourg	FR	TOP_SRAM2x15x16x8_with_FILL	I	
IPHC-Univ. Louis Pasteur	Strasbourg	FR	TopSensor_10u_12u_25u	I	
2 Institution(s)			**14 Circuit(s)**		

SA35C10_3
Technology: austriamicrosystems 0.35 µm CMOS C35B4C3
Starting date: 05 October 2010
Delivery of chips: 25 November 2010

Institution	Town	Country	Top Cell	E R I	Function
LETI/CEA	Grenoble	FR	CINESIC_32V_A	R	ASIC for a 32-channels-neuronal-signals-recording implant.
1 Institution(s)			**1 Circuit(s)**		

austriamicrosystems 0.35 µm CMOS RF

A35R10_1
Technology: austriamicrosystems 0.35 µm CMOS RF C35B4M3
Starting date: 01 March 2010
Delivery of chips: 25 May 2010

Institution	Town	Country	Top Cell	E R I	Function
ENSERG	Grenoble	FR	final_masque_IMEP_2010	R	Transmission Lines.
IneSS	Strasbourg	FR	ECG_HALL	R	The circuit is intended for ECG and magnetic field measurement with Hall effect devices.
National University of Singapore	Singapore	SG	GyroLayoutTapeOut	ER	MEMS Gyroscope drive and sense circuit.
Mikroelektronik Arastirma Gelistirme Tasarim ve Ticaret Limited Sirketi	Istanbul	TR	FDESEN	RI	The IC contains high frequency passive filter blocks.
4 Institution(s)			**4 Circuit(s)**		

A35R10_2
Technology: austriamicrosystems 0.35 µm CMOS RF C35B4M3
Starting date: 07 June 2010
Delivery of chips: 17 August 2010

Institution	Town	Country	Top Cell	E R I	Function
ENSEA	Cergy Pontoise	FR	Octo_v2_1	R	Branch line coupler, calibration motifs.
1 Institution(s)			**1 Circuit(s)**		

A35R10_3
Technology: austriamicrosystems 0.35 µm CMOS RF C35B4M3
Starting date: 06 September 2010
Delivery of chips: 16 November 2010

Institution	Town	Country	Top Cell	E R I	Function
ENSIEG	Saint Martin d'Hères	FR	puce_equilibrage_v1	R	Integrated equiliber for battery pack; Application in power conversion.
EDA Solutions Limited	Fareham	UK	Alphatestv1_top_R5	R	Test chip to prove IC design capability/methodology for customer of EDA Solutions in UK.
2 Institution(s)			**2 Circuit(s)**		

SA35R10_1
Technology: austriamicrosystems 0.35 µm CMOS RF C35B4M3
Starting date: 01 June 2010
Delivery of chips: 03 August 2010

Institution	Town	Country	Top Cell	E R I	Function
LETI/CEA	Grenoble	FR	ACTINA2	R	
1 Institution(s)			**1 Circuit(s)**		

austriamicrosystems 0.35 µm SiGe

A35S10_1
Technology: austriamicrosystems 0.35 µm SiGe S35D4M5
Starting date: 01 March 2010
Delivery of chips: : 03 May 2010

Institution	Town	Country	Top Cell	E R I	Function
University of Adelaide	Adelaide	AU	chip_tc2_tapeout	R	L-Band Radio Riceiver Array chip.
ENST Bretagne	Brest	FR	anadec	R	Analogue decoder, test for parasitic elements correction.
University of Southampton	Southampton,	UK	prw_mar_2010	E	7 GHz Oscillator.
MOSIS	Marina del Rey	US	V02SAA	R	High dynamic range charge integrator for high energy physics experiments.
4 Institution(s)			**4 Circuit(s)**		

A35S10_2
Technology: austriamicrosystems 0.35 µm SiGe S35D4M5
Starting date: 07 June 2010
Delivery of chips: 20 September 2010

Institution	Town	Country	Top Cell	E R I	Function
MIND	Archamps	FR	TARANIS_A2	R	Multi channel charge amplifier circuit for the analysis of radiations from lightnings and sprites.
LAL/Université Paris Sud	Orsay	FR	microroc	R	MICROROC (MICROmegas ReadOut Chip) is the very front end chip designed in BiCMOS SiGe 0.35µm technology for the readout of the Micromegas foreseen for the Digital Hadronic CALorimeter (DHCAL) of the future International Linear Collider. MICROROC readout is a semi-digital readout with 2 thresholds wich allows both good tracking and coarse energy measurement. It also integrates on chip data storage.
IneSS	Strasbourg	FR	TOP_FAMOSI_3_SF	R	
IneSS	Strasbourg	FR	TOP_FAMOSI_3_TIA	R	
INP Lyon/IN2P3	Villeurbanne	FR	DSm	R	Read-out system of detection and measure of charges in the range of [2pC-10pC]. A test of a low quiescent current buffer is also present in the circuit.
Mikroelektronik Arastirma Gelistirme Tasarim ve Ticaret Limited Sirketi	Istanbul	TR	ADC8015_1p2_DUAL_TOP	I	The IC is a high speed ADC (Analog to Digital Converter).
5 Institution(s)			**6 Circuit(s)**		

A35S10_3
Technology: austriamicrosystems 0.35 µm SiGe S35D4M5
Starting date: 06 September 2010
Delivery of chips: 16 November 2010

Institution	Town	Country	Top Cell	E R I	Function
MOSIS	Marina del Rey	US	V08uaa	R	
1 Institution(s)			**1 Circuit(s)**		

A35S10_4
Technology: austriamicrosystems 0.35 µm SiGe S35D4M5
Starting date: 22 November 2010
Delivery of chips: 21 February 2011

Institution	Town	Country	Top Cell	E R I	Function
MIND	Archamps	FR	INSMEDI_A1	I	
ENSEA	Cergy Pontoise	FR	1_Extra_elements	ER	Part of a frequency synthesizer + Test designs.
Thales SA	Elancourt	FR	TOP_ARAMIS_AA	I	
CEA-SACLAY	Gif sur Yvette	FR	SCOTT_2	R	
CMP	Grenoble	FR	top_PV_no_ESD_run3	R	
CMP	Grenoble	FR	TOP_PV_S35	R	
LPSC/IN2P3	Grenoble	FR	chip_mimac_64_v3c	R	
University of Southampton	Southampton	UK	uksp_nov_2010	E	Oscillator and Photonics Driver Amplifier.
UC Lawrence Berkeley National Lab.	Berkeley	US	HERMES64	R	This is a 64 channel IC for readout of micro channel plate detectors. The application is for scientific research of plasma in space aboard a multi-national space agency collaboration satellite to be sent to Mercury (BepiColombo mission).
8 Institution(s)			**9 Circuit(s)**		

SA35S10_1
Technology: austriamicrosystems 0.35 µm SiGe S35D4M5
Starting date: 19 March 2010
Delivery of chips: 02 July 2010

Institution	Town	Country	Top Cell	E R I	Function
LAL/Université Paris Sud	Orsay	FR	hardroc2b	I	
LAL/Université Paris Sud	Orsay	FR	maroc3	I	
LAL/Université Paris Sud	Orsay	FR	skiroc2	I	
LAL/Université Paris Sud	Orsay	FR	spaciroc	I	
LAL/Université Paris Sud	Orsay	FR	spiroc_little	I	
LAL/Université Paris Sud	Orsay	FR	spiroc2a	I	
LAL/Université Paris Sud	Orsay	FR	spiroc2b	I	
1 Institution(s)			**7 Circuit(s)**		

austriamicrosystems 0.35 µm High Voltage

A35V10_1

Technology: austriamicrosystems 0.35 µm High Voltage H35B4D3
Starting date: 15 February 2010
Delivery of chips: 23 April 2010

Institution	Town	Country	Top Cell	E R I	Function
CMC/Queen's University	Kingston	CA	ICMTRAAK	R	A segmented gate driver is designed to adjust the driving capability of the gate driver in order to improve the conversion efficiency for a wide rang of loads.
CMC/Queen's University	Kingston	CA	ICMTRRIS	R	Integrated High and Low Side High Voltage High Power Power Stage and Driver for SMPS.
Thales SA	Elancourt	FR	TOP_TRANS_AA	I	
LAAS	Toulouse	FR	autosens01	R	Power management circuit for energy scavenging.
MOSIS	Marina del Rey	US	V02HAA	R	High voltage and high current function generator. Maximum output voltage is 18 V and maximum output current is 5 mA for each output PAD.
4 Institution(s)			**5 Circuit(s)**		

A35V10_2

Technology: austriamicrosystems 0.35 µm High Voltage H35B4D3
Starting date: 26 April 2010
Delivery of chips: 09 July 2010

Institution	Town	Country	Top Cell	E R I	Function
NEURELEC	Vallauris	FR	Ring_CAFE24	I	It's a neural stimulator.
Hong Kong U. of Sc. & Techno	Kowloon	HK	SISO_BOOST	ER	An single input single boost mode power converter for academic research.
University College London	London	UK	DBS_IC_chip_final_v2	R	Stimulator chip for a biomedical application.
3 Institution(s)			**3 Circuit(s)**		

A35V10_3

Technology: austriamicrosystems 0.35 µm High Voltage H35B4D3
Starting date: 09 August 2010
Delivery of chips: 21 October 2010

Institution	Town	Country	Top Cell	E R I	Function
ENSIEG	Saint Martin d'Hères	FR	puce_cde_v2	R	The circuit contains 12 legs of inverter including the commandes. It could serve to driver power switches in several topologies. This circuit contains 12 legs of inverter including the commands. It could serve to driver power switches in several topologies.
ENSEEIHT	Toulouse	FR	photo_asic	R	The ASIC is composed of various optoelectronic components, 5 CMOS avalanche photodiodes (APDs), a MSM photoconductor and a schottky photodiode are implemented. One of the APDs is also implemented with its instrumentation circuit. Furthermore, an APDs array constituted of 16 pixels are present. Each APD is individually biased and instrumented. The ASIC is composed of various optoelectronic components. 5 CMOS avalanche photodiodes (APDs), a MSM phtoconductor and a schottky photodiode are implemented. One of the APDs is also implemented with its instrumentation circuit. Furthermore, an APDs array constituted of 16 pixels are present. Each APD is individually biased and instrumented.
2 Institution(s)			**2 Circuit(s)**		

A35V10_4

Technology: austriamicrosystems 0.35 µm High Voltage H35B4D3
Starting date: 08 November 2010
Delivery of chips: 28 January 2011

Institution	Town	Country	Top Cell	E R I	Function
LIRMM	Montpellier	FR	cafe12_V2_1	R	Functional Electrical Stimulator.
UC Lawrence Berkeley National Lab.	Berkeley	US	FCCDSF_TOP	I	Low impedance buffer for fast CCD readout.
MOSIS	Marina del Rey	US	V0BDAA	R	Lab-on-chip platform; chemical droplet transport achieved via electrowetting requiring application of high electric field to a droplet to induce movement.
3 Institution(s)			**3 Circuit(s)**		

STMicroelectronics 130 nm CMOS

S13C10_1
Technology: STMicroelectronics 130 nm CMOS HCMOS9GP
Starting date: 10 February 2010
Delivery of chips: 15 June 2010

Institution	Town	Country	Top Cell	E R I	Function
LETI/CEA	Grenoble	FR	LETIBEE_V1_6	I	SoC including and ultra-low power IEEE 802.15.4 (Zigbee) compliant transceiver and 8051 microcontroller.
LETI/CEA	Grenoble	FR	UWBNanocomV1	I	RF front-end for Ultra Wide Band receiver, including LNA, mixers, integrators, ADCs, digital and frequency synthesis.
IMS	Talence	FR	LNAVLPULP	R	This die contents LNAs at 2.4 G for low power applications.
Università degli studi di Pavia	Pavia	IT	pcm_top	R	Generation of current references.
3 Institution(s)			**4 Circuit(s)**		

S13C10_2
Technology: STMicroelectronics 130 nm CMOS HCMOS9GP
Starting date: 07 April 2010
Delivery of chips: 22 July 2010

Institution	Town	Country	Top Cell	E R I	Function
University of Seville - Escuela Superior de Ingenieros	Sevilla	ES	Chip_VGA_FILTRO	R	VGA and filter for ULP Bluetooth baseband applications.
IMS	Talence	FR	DROUJB	R	Delta sigma ADC with 4th order resonator, sampling frequency : 4 GHz, 3 bits output.
University of Virginia	Charlottesville	US	UVA_MOUSE_TPv1	R	Experimental wireless temperature sensor.
3 Institution(s)			**3 Circuit(s)**		

S13C10_3
Technology: STMicroelectronics 130 nm CMOS HCMOS9GP
Starting date: 08 June 2010
Delivery of chips: 17 November 2010

Institution	Town	Country	Top Cell	E R I	Function
UCL, Lab. Microelectronique	Louvain la Neuve	BE	UCL0610	R	DC/DC converter, opamp, devices.
ETH Zentrum IIS	Zurich	CH	DAC15	R	High-performance digital-to-analogue converter (DAC).
ETH Zentrum IIS	Zurich	CH	ETH_YCHEN_SYN	R	High performance frequency synthesizer for RF applications.
Instituto Microelectronica Sevilla (IMSE)	Sevilla	ES	BTLE_TRX	E	A Bluetooth Low Energy transceiver working at 2.4 GHz for biomedical applications.
University of Seville - Escuela Superior de Ingenieros	Sevilla	ES	Chip_tesis	R	VGA and filter for ULP Bluetooth baseband applications.
CMP	Grenoble	FR	TOP_COMMUN	R	
LETI/CEA	Grenoble	FR	AUTOMATCH_2p4	R	The designed circuit is able to automatically match antenna impedance (version with PA and RF Filter).
LETI/CEA	Grenoble	FR	AUTOMATCH_MStd	I	The designed circuit is able to automatically antenna impedance (version without PA and RF Filter.
LETI/CEA	Grenoble	FR	BATRF_V1	I	UWB transceiver SOC design for low-power low-data-rate applications in the 4-to-5GHz band. It includes, as a receiver, the XNOR-based energy detector and as a transmitter, a flexible pulse generator. Each part of the circuit can operate separately with its own programmable IOs in such a way that the chip can behave either like a complete IEEE 802.15.4a compliant transceiver.
LETI/CEA	Grenoble	FR	CGAB_LNA_TOP	I	Inductorless ultra low power LNA.
LETI/CEA	Grenoble	FR	ImageurTHz3	R	CMOS Terahertz detectors ; test structures consisting of differently sized MOSFETs, coupling antennas, integrated amplifiers, and multiplexing circuitry.
ENSSAT/Université Rennes 1	Lannion	FR	ochrev2_chip	R	This chip implements new hybrid RNG (Random Number Generator) composed of True Random Number Generators (TRNGs) and Pseudo Random Number Generators (PRNGs). The TRNGs randomness quality are monitored on real-time by hardware statistical tests. The design is able to detect TRNGs weaknesses due to defects or to non-invasive attacks.
L2MP POLYTECH Marseille	Marseille	FR	rfidcapt	R	Pulse Generators / Energy Detectors/RFID front

					end.
L2MP POLYTECH Marseille	Marseille	FR	TOP_CMP10A_lvs	R	Energy Detectors/Demodulator.
LIRMM	Montpellier	FR	TOP_FPGA	R	Magnetic non volatile FPGA.
UPMC Paris 6	Paris	FR	SDM_2P4GHz	R	Sigma Delta modulator that works at 2.4 GHz.
UPMC Paris 6	Paris	FR	SDM_900MHz	R	Sigma Delta modulator that works at 900 MHz.
IMS	Talence	FR	NISS	R	This circuit is a delay oriented design (DOD) frequency synthesizer based on a mixed Delay Locked Loop (DLL) and Phase Locked Loop architecture (PLL). This circuit is reconfigurable and is able to work from 1 to 3 GHz.
University of Modena & Reggio Emilia	Modena	IT	UniMore_2010	R	Down-conversion mixer. I/Q Demodulator. Frequency Doubler.
ETRI	Gwangju	KR	ETRI_1006	R	Together with a photodiode, the circuit is used to receive 10.3 Gb/s continous wave optical signal.
Linköping University - ISY	Linköping	SE	saradc10bv0	R	A 10-bit Ultra-Low Power Successive-Approximation ADC.
14 Institution(s)			**21 Circuit(s)**		

S13C10_4
Technology: STMicroelectronics 130 nm CMOS HCMOS9GP
Starting date: 15 September 2010
Delivery of chips: 09 February 2011

Institution	Town	Country	Top Cell	E R I	Function
ETH-Zentrum	Zurich	CH	ETH_CurrentPipe	R	ETH-CurrentPipe is a prototype of a simple pipeline analog-to-digital converter based on current mirrors. It is designed for 10 MS/s and 10 bit resolution. It is used as a proof of concept only.
Instituto Microelectronica Sevilla (IMSE)	Sevilla	ES	POWDERS_1	R	Neural recording channel with feature extraction capabilities.
Aalto University	Espoo	FI	iradsar2	R	Multi-band X/L/C rf receiver with ADC.
SUPELEC	Gif sur Yvette	FR	MNEMS	R	NEMS oscillator feedback loop (ANR-funded M&NEMS project). (Capacitive detection and pulsed electrostatic actuation).
LETI/CEA	Grenoble	FR	TXBBFILT	I	This chip is composed of an analog pulse generator for 3-5 GHz UWB band. It uses analog filter impulse response.
LETI/CEA	Grenoble	FR	TXOSCQ	I	This chip is composed of a new pulse generator for 3-10 GHz UWB band. It is based on a controlled oscillator.
LETI/CEA	Grenoble	FR	TXPULSYN	I	This chip is composed of a digital pulse generator for 3-5 GHz UWB band. It is based on pulse recombination.
LETI/CEA	Grenoble	FR	UMETAG41	I	High data rate communication interface for wireless NV-Memory applications.
Chalmers University of Technology	Gothenburg	SE	flexsoc_top	R	The FlexCore processor uses a flexible interconnect instead of a pipeline to connect all parts to the data path. Each data path unit is linked to every other unit, this allows for a more flexible scheduling which leads to reduced cycle count. A full interconnect provides flexibility but is costly in area and power.
Linköping University - ISY	Linköping	SE	25GHzPA_core	R	This is a design of a 25 GHz Class A Power Amplifier with output power of ~11dBm.
Linköping University - ISY	Linköping	SE	PADOVA_HP	R	CMOS RF power amplifier for wireless communication.
Columbia University	New York	US	deliriem	R	An ultra low power audio frequency asynchronous ADC with automatic digital calibration and signal adaptive biasing. An on-chip 5kb RAM allows the user to program arbitrary quantization transfer functions. The chip communicates over an SPI bus.
8 Institution(s)			**12 Circuit(s)**		

S13C10_5
Technology: STMicroelectronics 130 nm CMOS HCMOS9GP
Starting date: 24 November 2010

Institution	Town	Country	Top Cell	E R I	Function
CIM-PACA	Biot	FR	CIMPACA_2010	R	2.45 GHz transmitter for cochlear implant application.
Université de Bourgogne	Dijon	FR	Retine_Var	R	This circuit is based on a new approach for movement detection from an optical scene using variance of pixels. The purpose of this circuit is to characterize this new approach in CMOS 0.13um.
LETI/CEA	Grenoble	FR	CGABV2	I	Inductorless ultra low power LNA.
LETI/CEA	Grenoble	FR	UWBRXSWV	I	This chip is a UWB receiver based on a double I/Q architecture.
L2MP POLYTECH Marseille	Marseille	FR	CMP10B	R	UWB Pulse Generators/VCO/.
Linköping University - ISY	Linköping	SE	LDA	R	Wide band low noise low distortion amplifier for

					wireless applications.
5 Institution(s)			**6 Circuit(s)**		

STMicroelectronics 130 nm SiGe

S13S10_1
Technology: STMicroelectronics 130 nm SiGe BiCMOS9MW
Starting date: 10 February 2010
Delivery of chips: 30 June 2010

Institution	Town	Country	Top Cell	E R I	Function
Peraso Technologies, Inc.	Toronto	CA	PRS1013A1	I	60 GHz transceiver prototype circuit.
Peraso Technologies, Inc.	Toronto	CA	PRS1013A1B0	I	Test structures and breakouts of sub-blocks for a 60 Ghz transceiver circuit.
IMS	Talence	FR	CODESIGN	R	Power Amplifier and Antenna for illimeter-wave applications.
IMS	Talence	FR	DUNG	R	Double-balanced mixer with integrated transformers for millimeter-wave applications.
IMS	Talence	FR	LNARS	R	Low Noise Amplifier for millimeter-wave applications.
IMS	Talence	FR	Trmmw10	R	Set of passive components designed for operation in mm-wave frequencies. This set includes 11 integrated transformers as well as de-embedding structures. The transformers differ in their topology, dimensions and transformation ratio.
IMS	Talence	FR	VCOLNA	R	Low Noise Amplifier and Voltage Controlled Oscillator for millimeter-wave applications.
LAAS	Toulouse	FR	LAAS_VELO0210	R	79 GHz double-balanced direct down-converter for the ANR VeLO project.
LAAS	Toulouse	FR	SP51_VELO0210	R	79 GHz receiver containing a LNA, a double-balanced direct down-converter and a VCO for th ANR VeLO project.
LAAS	Toulouse	FR	SP52_VELO0210	R	79 GHz receiver containing the integrated patch antenna followed by the LNA, a double-balanced direct down-converter and a VCO for the ANR VeLO project.
BWRC	Berkeley	US	TUSI_TRX1	R	Circuit to test components for a 94 GHz transceiver: LNA, mixer, PLL, DLL VCO, VCo buffers and pulsed power-amplifier.
4 Institution(s)			**11 Circuit(s)**		

S13S10_3
Technology: STMicroelectronics 130 nm SiGe BiCMOS9MW
Starting date: 08 June 2010
Delivery of chips: 22 October 2010

Institution	Town	Country	Top Cell	E R I	Function
University of Toronto	Toronto	CA	sens_ant	R	120 GHz sensor for distance measurement applications. The chip is developed in cooperation with Robert Bosch GmBH.
University of Toronto	Toronto	CA	sens_brk	R	120 GHz sensor breakouts.
Thales S.A.	Elancourt	FR	EB1_AA	I	Test of microwave devices.
Thales S.A.	Elancourt	FR	EBDMUX_AA	I	Demultiplexor and sampler.
IMS	Talence	FR	SAFEWAVE	R	Radio-frequency Front-end (RFFE) dedicated to automotive radar applications (77 GHz). This circuit integrates the main building-blocks of a RFFE (LNA, VCO and Mixer).
Catena Holding B.V..	Delft	NL	SIAM_TS2_TOP	R	Low-Noise Amplifier and Voltage Controlled Oscillator for 60 GHz wireless applications.
Delft University of Technology	Delft	NL	TUDYLDY	R	Test of devices : - frequency doubler, power amplifiers, LNA, 100 GHz band filter, mixer, receiver front end, power combiners TRL de-embedding standards.
Delft University of Technology	Delft	NL	TUMEMPHIS1	R	Radar imaging for civil application;
Philips Research	Eindhoven	NL	PhilipsTop	R	60 GHz transceiver building blocks such as PA, PA-modulator, VCO, PLL.
BWRC	Berkeley	US	TUSI_SA1	R	Standalone structures of distributed amplifier (DA) and 94 GHz PLL to be used in 94 GHz transceiver for medical imaging.
BWRC	Berkeley	US	TUSI_TRX2	R	Circuit consists of a 94 GHz transceiver with pulsed functionality. The goal is for medical imaging or very high speed UWB communications.
7 Institution(s)			**11 Circuit(s)**		

S13S10_4
Technology: STMicroelectronics 130 nm SiGe BiCMOS9MW
Starting date: 15 September 2010
Delivery of chips: 31 January 2011

Institution	Town	Country	Top Cell	E R I	Function
University of Toronto	Toronto	CA	UTDBTXRX	R	160 GHz wireless transceiver with on-chip antennas and integrated PLL.
1 Institution(s)			**1 Circuit(s)**		

S13S10_5
Technology: STMicroelectronics 130 nm SiGe BiCMOS9MW
Starting date: 24 November 2010

Institution	Town	Country	Top Cell	E R I	Function
University of Calgary	Calgary	CA	U2DKMFLNA	R	This circuit is a design of Low Noise Amplifiers. The design started by extracting a small-signal electrical and noise lumped circuit model for SiGe bipolar transistors. The model is used to design a theoretical optimization technique for achieving very low noise figure amplifiers. The technique is verified in simulation using 0.12um BiCMOS technology and now it will be verfied through measurement of these fabricated chips.
University of Toronto	Toronto	CA	ISL_BIC_OPTO1	R	The circuit is an optoelectronic receiver, and will be used to test the responsivity and bandwidth of various photodetector topologies in a standard BiCMOS process.
California Institute of Technology	Pasadena	US	CITST1	R	Circuits are low noise amplifiers and transistors for use in ground-based radio-astronomy research.
3 Institution(s)			**3 Circuit(s)**		

SS13S10_1
Technology: STMicroelectronics 130 nm SiGe BiCMOS9MW
Starting date: 01 September 2010
Delivery of chips: 10 October 2010

Institution	Town	Country	Top Cell	E R I	Function
Peraso Technologies, Inc.	Toronto	CA	CMP_S13S101R5	I	60GHz transceiver prototype circuit.
Peraso Technologies, Inc.	Toronto	CA	CMP_S13S101R6	I	Test structures and breakouts of sub-blocks for a 60GHz transceiver circuit.
1 Institution(s)			**2 Circuit(s)**		

STMicroelectronics 65 nm CMOS

S65C10_1
Technology: STMicroelectronics 65 nm CMOS CMOS065
Starting date: 28 April 2010
Delivery of chips: 30 August 2010

Institution	Town	Country	Top Cell	E R I	Function
UCL, Lab. Microelectronique	Louvain la Neuve	BE	UCL0410_ANRF	R	Low-power OTA, UWB pulse generator and ring oscillators.
University of Macau	Macau SAR	CN	PPTX	R	A polyphase transmitter front-end for cognitive radio applications. It consists of two lowpass filters, a set of polyphase mixers, a multi-phase signal generator and a driver amplifier.
University of Paderborn	Paderborn	DE	gpvliw_cpu_control_pads	R	This circuit implements a 4-issue VLIW process dedicated for baseband and multimedia applications. Maximum frequency is about 300 MHz.
University of Wuppertal	Wuppertal	DE	UNIWUP	R	Circuits are part of an University Interaction with STMicroelectronics. Circuit is used for research on THz Imaging using CMOS65nm technlology.
LETI/CEA	Grenoble	FR	DIGBEE_V1	R	DIGBEE is a digitizing and sampling circuit that will be used in an ultra low power radio receiver. Goals are to digitize the RF signal at the very first stages of the reception chain ans to under-sample the signal at high IF; A bi-standard Zigbee Bluetooth transceiver will be one of its applications.
LETI/CEA	Grenoble	FR	UAR	R	This circuit is a UWB receiver based on a new digital approach. Thanks to this approach an inductorless continuous tim FIR filter has been implemented to achieve adaptive blocker rejection in a IR-UWB non coherent receiver.
MENTA	Montpellier	FR	MNT_eFPGA_wrapper	R	
IMS	Talence	FR	HSFDScascode	R	Power amplifier for Wifi applications;
IMS	Talence	FR	KAMAL	R	Switch RF (TX/RX) for WCDMA applications.
IMS	Talence	FR	NANOSPACE	R	NANOSPACE is a multipartner test chip for advanced investigation of possible failure mechanisms in deep submicron technologies in the context of long-term missions. It includes

					various test structures for characterizing the effect of ageing on radiation, EMC and ESC robustness, and for demonstrating different optical failure localization techniques.
LAAS	Toulouse	FR	LAAS_ACC_DAC	R	The submitted GDS contains two main blocks of a DDs-based UWB transmitter: - the phase accumulator, - the digital/analog converter.
LAAS	Toulouse	FR	RECEIVER60GHz	R	- 60 GHz ultra-wideband receiver; - 60 GHz low noise amplifier. - 60 GHz test structures.
LAAS	Toulouse	FR	TRANSMITTER60GHZ	R	- 60 GHz ultra-wideband transmitter (including VCo, mixer and PA).
LAAS	Toulouse	FR	UPMIXERLNA	R	- 60 GHz up-mixer. - 60 GHz power amplifier. - 60 GHz test structures.
University of Michigan	Ann Arbor	US	Michigan65_FFT	R	Energy-efficient, medium performance, ultra-low voltage signal processing core.
BWRC	Berkeley	US	bwrc_bb60ghz_rx_v2	R	This chip contains the circuitry for an adaptive 10Gb/s 60GHz baseband, containing a 40-tap complex. Decision Feedback Equalizer (DFE), Clock & Data Recovery (CDR) and Variable Gain Amplifier (VGA).
BWRC	Berkeley	US	RFID	R	The chip implements an ultra-low power active RFID tag that is energy autonomous and operates in the ISM 2.4GHz band.
BWRC	Berkeley	US	trans60ph_1	R	This chip consists of LNA, Quadrature mixer, Hybrid, Phase-rotator, PLL, LO distribution network, high-speed modulator and switching PA.
BWRC	Berkeley	US	WIBI_ENTX	R	This chip contains an prototype for energy neutral wireless link for implantable biomedical applications; It consists of a RF to DC conversion block enabeling wireless transfer and a passive transmitter for the data link.
MIT	Cambridge	US	lvsoc_s5_finish	R	Expirimental low-power microcontroller.
UCLA	Los Angeles	US	Flash_VW	R	Variation-tolerant Flash ADC.
UCLA	Los Angeles	US	FPGA_ST65_MAY10_TOP	ER	Field Programmable Gate Array.
UCLA	Los Angeles	US	Tx_DFE	R	Digital front-end (DFE) implementation of LTE/WiMAX transmitter. The circuit contains the digital components required for enabling a Tx DFE.
12 Institution(s)			**23 Circuit(s)**		

S65C10_2
Technology: STMicroelectronics 65 nm CMOS CMOS065
Starting date: 09 June 2010
Delivery of chips: 03 December 2010

Institution	Town	Country	Top Cell	E R I	Function
Columbia University	New York	US	CU_UWBRX_09RS	R	This circuit implements an ultra low power receiver operating on the UWB 3.1-5Ghz. by using impulse radio and occupying a wide band (>500
California Institute of Technology	Pasadena	US	CALTECH_MICS	R	Implementing a process-variation-tolerant technique for an analog circuits used in a biomedical implant; A high data rate optical receiver for short-haul and chip-to-chip interconnects.
2 Institution(s)			**2 Circuit(s)**		

S65C10_3
Technology: STMicroelectronics 65 nm CMOS CMOS065
Starting date: 29 November 2010

Institution	Town	Country	Top Cell	E R I	Function
University of Macau	Macau SAR	CN	DC20101129Chip1	R	High Speed Low Power ADC for Mobile TV application.
University of Macau	Macau SAR	CN	DC20101129Chip2	R	High Speed Low Power ADC for Mobile TV application.
University of Macau	Macau SAR	CN	DC20101129Chip3	R	High Speed Low Power ADC for Mobile TV application.
University of Paderborn	Paderborn	DE	gpvliw_cpu_control_pads	R	General purpose, ultra-low power RISC processor cores dedicated for energy constrained applications implemented in subthreshold technology. Wide ranges of supply voltage and clock frequency supported.
Universitat politechnica de Catalunya	Barcelona	ES	CONF_LNA	R	The chip includes the design of two inductorless wideband LNA\'s and one mixer, including buffer for measurement purposes. The circuit main purpose is to have tunability to change ist specifications depending on the needs of a given front-end.

Universitat politechnica de Catalunya	Barcelona	ES	LNA_PVT_2	R	A Low-Power Noise Amplifier robust to PVT variations. The die contains the amplifier and additional support circuitry for PVT compensation, on-chip monitoring (BIT capability) and auxiliary circuitry for test and characterization.
Universidad Carlos III de Madrid	Madrid	ES	ADC_all_v02	R	Analog to Digital converter for comunications. Using a time-resolution quantizer and a sigma-delta modulator.
VTT Information Technology	Espoo	FI	VTT_65_02	R	Millimeter-wave low noise amplifier, millimeter-wave receiver, test structures.
Ecole Centrale de Lyon	Ecully	FR	cmos_chip_top	R	Transmission and reception paths for optical interconnect including control and test circuitry. Note: CMOS die will be bonded to a photonics die (dimensions will be specified, no packaging required).
ENSSAT - Univ. Rennes	Lannion	FR	express_chip_top	R	Power gated transceiver for wireless sensor network (to be completed).
INVIA	Meyreuil	FR	tc_top	I	Analog testchip in 65nm technology.
IMS	Talence	FR	ADLIC	R	This circuit is an Analog-to-Digital Converter with a Flash architecture and 3 bits resolution. Signal and Clock inputs are differential. The maximum input and sampling frequencies are 8Ghz. The 3 bits are demultiplexed (in-chip) by 4 and the outputs follow the LVDS standard.
IMS	Talence	FR	FULLQSTREAM	R	A power Amplifier (PA) dedicated for 60Ghz WPAN applications. This work is in the frame of the MEDEA+QSTREAM project that aims at achieving a high saturated power of 15dBm. The PA is based on current and voltage combining techniques at the input and the output, respectively. Hence, a splitter, baluns and distributed active transformers are integrated on chip. The PA targets 16dBm of saturated power (Psat) with a Power Added Efficiency (PAE) of 10%.
IMS	Talence	FR	MIXTE	R	This chip contains different passive devices customized to operate at mmW frequencies. Baluns and transformers with their de-embedding structures are included to characterize their capability of converting single to differential mode. Those devices are scheduled to be integrated in active circuits such as power amplifiers (PA), low noise amplifier (LNA). Additionally, a frequency divider 1/2-(60GHz), is also integrated to be used in a PLL.
LAAS	Toulouse	FR	LAAS_ACC_DAC	R	The submitted GDS contains two main blocks of a DDS-based UWB transmitter. - Phase accumulator, - the digital/analog converter.
LAAS	Toulouse	FR	LAAS_DCPT_ZF	R	The submitted GDS contains two main blocks of a DDS-based UWB transmitter. - Phase accumulator, - the digital/analog converter.
LAAS	Toulouse	FR	LAAS_ROM_SEQ	R	The submitted GDS contains two main blocks of a DDS-based UWB transmitter. - Phase accumulator, - the digital/analog converter.
LAAS	Toulouse	FR	VCOSPLITTER	R	- 60GHz splitter. - 60GHz test structures.
Tyndall National Institute	Cork	IE	TopMorpheus	R	40G VCSEL driver.
Università di Padova	Padova	IT	SKURAD	R	Microwave imaging for medical applications.
Linköping University - ISY	Linköping	SE	PADOVA_LP	R	CMOS RF power amplifier for wireless communication.
Linköping University - ISY	Linköping	SE	pipelineLpTop	R	A high-speed Low-Power 8-bit Pipelined ADC.
Linköping University - ISY	Linköping	SE	SDM_ULP_chip11_PAD	R	Sigma delta modulator for low power application.
Lund University	Lund	SE	eitnov10a	R	iterative Decoder & Digital Filter.
Lund University	Lund	SE	eitnov10b	R	Cellular transmitter circuit.
Lund University	Lund	SE	eitnov10c	R	Analog Decoder. Delta Sigma AD.
Lund University	Lund	SE	eitnov10d	R	Delta Sigma ADs.
Lund University	Lund	SE	eitnov10e	R	Mixer, Low Power FE, Adder.
BWRC	Berkeley	US	bwrc_tisar	R	Time-interleaved successive approximation analog-to-digital converter (SAR ADC) with mixed-mode calibration of channel mismatches and static nonlinearities. The circuit consists of 30 analog SAR ADC channels (including dummy and reference channels), digital calibration and control logic, and memory buffer for testing purposes. Expected sampling frequency, effective resolution, and power are 3GS/s, 8 bits, and 20mW, respectively.
University of Minnesota	Minneapolis	US	BUDAPEST_FULLCHIP	ER	University research ideas on embedded cache memory and on-chip reliability monitor circuits.
California Institute of	Pasadena	US	Receiver_Final	R	Receiver for high speed interconnects. It

Technology					includes a clock recovery PLL with low jitter and power.
Carnegie Mellon University	Pittsburgh	US	CHIP_TOP_FLOORPLAN	R	University research testchip with multiple experiments. There is a SRAM block with multi-bit ECC, logic and wire test structures for low temperature operation, and physically unclonable functions.
19 Institution(s)			**32 Circuit(s)**		

STMicroelectronics 65 nm SOI

S65I10_1
Technology: STMicroelectronics 65 nm SOI CMOS065-SOI
Starting date: 03 June 2010
Delivery of chips: 30 September 2010

Institution	Town	Country	Top Cell	E R I	Function
LETI/CEA	Grenoble	FR	GPULSE	R	The GPULSE circuit implements a complete 60GHz transceiver for high data-rate/low-power communications. It uses a impulse emission and enveloppe detection method that enables to achieve up to 2.5Gbit/sec with less than 80mW consumption. Applications: fast down-loading.
LETI/CEA	Grenoble	FR	GPULSE_ANT	R	The GPULSE-ANT circuit implements a complete 60GHz transceiver for high data-rate/low-power communications; It uses a impulse emission and evelope detection method that enables to achieve up to 2.5Gbit/sec with less than 80mW consumption. The circuit implements also integrated antennas at the 60GHz band; Applications: fast down-loading.
LETI/CEA	Grenoble	FR	GTIME	R	This circuit manages the \"quench\" position and the communication rate for the GPULSE transceiver; The circuit is implemented in a stand alone version in order to validate the functionality.
LETI/CEA	Grenoble	FR	PYTHAGORAS	R	60GHz PLL for wireless HD and fast downloading fully compatible with the IEEE 802.15.3c standard.
LETI/CEA	Grenoble	FR	SWTL	R	Slow wave transmission lines test patterns for modeling and investigation of the slow wave lines at high frequency. Future applications: millimeter wave and terahertz circuits.
IMS	Talence	FR	LNAVCO60	R	60GHz VCO and LNA for WPAN application.
IEMN	Villeneuve d'Ascq	FR	IEMN-IR30G	R	Circuit designed in the framework of the SIAM project
IEMN	Villeneuve d'Ascq	FR	IEMN-IR60G	R	Circuit designed in the framework of the SIAm project.
IEMN	Villeneuve d'Ascq	FR	IEMN-SSB60G	R	Circuit designed in the framework of the SIAM project.
IEMN	Villeneuve d'Ascq	FR	IEMN-UP60G	R	Circuit designed in the framework of the SIAM project.
Delft University of Technology	Delft	NL	TUD_SIAM_SOI2	R	The function of this chip is : - 60GHz LNA - 60GHz mixer - 60GHz VCO - 60GHz integrated receiver front end - mm-wave N-way combining power amplifiers - Power combiners - TRL de-embedding standards.
ACREO AB	Norrkoping	SE	Acreo_SIAM_21GHz_bandpass_filter	R	This circuit is a 5th order Chebyshev 7 GHz bandpass filter designed for a 100 Gb/s SCM transceiver.
ACREO AB	Norrkoping	SE	Acreo_SIAM_21GHz_IQ_modulator	R	This circuit is a complete 21GHz broadband IQ modulator with filtering suitable for a 100 Gb/s optical transceiver.
ACREO AB	Norrkoping	SE	Acreo_SIAM_21GHz_mixer_testbench	R	This circuit is a 21 GHz broadband double balanced mixer with LO, RF and IF baluns suitable for a 100 Gb/s optical transceiver.
ACREO AB	Norrkoping	SE	Acreo_SIAM_7GHz_bandpass_filter	R	This circuit is a 5th order Chebyshev 7 GHz bandpass filter designed for a 100 Gb/s SCM transceiver.
ACREO AB	Norrkoping	SE	Acreo_SIAM_7GHz_IQ_modulator	R	This crictuit is a complete 7GHz broadband IQ modulator with filtering suitable for a 100Gb/s optical transceiver.
ACREO AB	Norrkoping	SE	Acreo_SIAM_7GHz_mixer_testbench	R	This circuit is a 7 GHz broadband double

					balanced mixer with LO, RF and IF baluns suitable for a 100 Gb/s optical transceiver.
ACREO AB	Norrkoping	SE	Acreo_SIAM_balun_testbench	R	This circuit is an active broadband balun suitab le for a 100 Gb/s SCM transceiver circuits.
ACREO AB	Norrkoping	SE	Acreo_SIAM_calibration_test_bench	R	This circuit is a testbench for performing de-embedding of RF-probes, analyzing Tx-lines, terminations and discrete components. There is a broadband single stage LNA test circuit also.
ACREO AB	Norrkoping	SE	Acreo_SIAM_LNA	R	This circuit is a 2-26 GHz broadband LNA suitable for a 100 Gb/s optical transceiver.
ACREO AB	Norrkoping	SE	Acreo_SIAM_passive_balun_testbench	R	This circuit is a passive balun for the LO signal for 7GHz and 21GHz mixers suitable for a 100 Gb/s optical transceiver.
ACREO AB	Norrkoping	SE	Acreo_SIAM_passive_combiner_testbench	R	This circuit is a passive combiner for the 7GHz and 21 GHz mixers suitable for a 100 Gb/s optical transceiver. The circuit includes a 7GHz and 21GHz IF balun also required for the mixers.
ACREO AB	Norrkoping	SE	Acreo_SIAM_quadrature_generator_testbench	R	This circuit is a passive quadrature generator for the LO signal at 7GHz and 21GHz for an IQ modulator suitable for a 100 Gb/s optical transceiver.
ACREO AB	Norrkoping	SE	Acreo_SIAM_RF_combiner	R	This circuit is a 2-26GHz broadband broadband active combiner (travelling wave amplifier) suitable for a 100 Gb/s optical transceiver.
ACREO AB	Norrkoping	SE	Acreo_SIAM_Sinc_bun_filter	R	This circuit is a 5th order Chebyshev 4.5GHz low pass filter designed for the output of a DAC for a 100 Gb/s SCM transceiver.
Ericsson AB	Stockholm	SE	EAB_IQ_demod	I	This circuit is a IQ demodulator designing for microwave assisted optical data communication system .
Ericsson AB	Stockholm	SE	EAB_Mixer1	I	SIAM project. This circuit is a down-conversion passive mixer design for microwave assisted optical data communication system.
Ericsson AB	Stockholm	SE	EAB_Mixer2	I	SIAM project. This circuit is a down-conversion passive mixer design for microwave assisted optical data communication system.
Ericsson AB	Stockholm	SE	EAB_Receiver	I	SIAM project. This project is a receiver design for microwave assisted optical data communication system.
Stanford University	Stanford	US	DynPipeADC	ER	This circuit is a low power analog-to-digital converter that targets a sampling rate of 500MS/s and resolution of better than 7 bits.
7 Institution(s)			**30 Circuit(s)**		

MEMSCAP 2.0 µm PolyMUMPS

M02P10_1
Technology: MEMSCAP 2.0 µm PolyMUMPS PolyMUMPS
Starting date: 05 January 2010
Delivery of chips: 06 April 2010

Institution	Town	Country	Top Cell	E R I	Function
CMC/Queen's University	Kingston	CA	IMUTRBBB	R	Our research objective is to provide a robotic cell microsurgery system that is able to extract Polar Body and Blastomere automatically with a silicon micro-knife to remove the required cells with minimum damage to a cell membrane. An ultrasonic cutting process will be introduced to the cell membrane.Touch and force sensors will be integrated to the micro-knife. By doing this, the whole process can be effectively automated.
CMC/Queen's University	Kingston	CA	IMUWTLLL	R	1- A chaotic micro resonator used for mass sensing. 2- A threshold-type mass sensor.
1 Institution(s)			**2 Circuit(s)**		

M02P10_2
Technology: MEMSCAP 2.0 µm PolyMUMPS PolyMUMPS
Starting date: 06 April 2010
Delivery of chips: 30 June 2010

Institution	Town	Country	Top Cell	E R I	Function
CMC/Queen's University	Kingston	CA	IMUICDM4	R	This is a compulsive force driven micromirror which will be used for CMC demo.
CMC/Queen's University	Kingston	CA	IMURNEDU	R	The applied space is for the graduate course "MEMS". 25 students are registered in this course for the winter 2010 term. A major project is required for this course, in which students will design a PolyMUMPS device. One or two best designs will be submitted for fabrication. Prototyping can really intrigue students.
CMC/Queen's University	Kingston	CA	IMURNMEM	R	The present project is to develop stiction-free cantilever or clamping-campling beams, which will not stick to the substrate during the releasing process and handling operation.
CMC/Queen's University	Kingston	CA	IMUSFBB2	R	We have a number of designs on this chip which we will test ot verigy our novel signal processing technique for coupled resonators. We also have devices to test the thermal response of microresonators as well as damping mechanisms affecting their operation.
1 Institution(s)			**4 Circuit(s)**		

M02P10_3
Technology: MEMSCAP 2.0 µm PolyMUMPS PolyMUMPS
Starting date: 06 July 2010
Delivery of chips: 01 October 2010

Institution	Town	Country	Top Cell	E R I	Function
CMC/Queen's University	Kingston	CA	IMUBCUCM	R	This relatively new technology that provides a means of transmitting and receiving ultrasonic waves has emerged as a leading research area in that the CMUT is able to achieve greater bandwidth and sensitivity than equivalent piezoelectric transducers, and better scaling laws that can lead to integration with CMOS and 3D imaging within small sizes.
CMC/Queen's University	Kingston	CA	IMUDTCV7	R	This chip builds on previous frictional conveyor design. The devices are designed to allow for large displacement platform manipulation with 3DOF, in conjunction with optical control feedback. The dynamic height adjustement is required to maximise the frictional contact between the sliding pad and the floating platform.
CMC/Queen's University	Kingston	CA	IMUDTCV8	R	This chip builds on previous frictional conveyor designs. The devices are designed to allow for large displacement platform manipulation with 3DOF, in conjunction with optical control feedback. This concept will allow for long range manipulation of objects regardless of geometric properties.
CMC/Queen's University	Kingston	CA	IMUDTVT2	R	The chip will investigated 2 DOF thermal actuators (TA) that can move in both vertical and lateral directions. Many designs have been proposed in the past of simple device being able to move either vertically or in-plane. A novel design being able to accomplish both of the aforementioned displacements will be designed and tested. These devices will also be implemented in simpler, longer range conveyors using the concept of lift and slide. FEA and macro model testing will be done beforehand to help assure successful designs.
CMC/Queen's University	Kingston	CA	IMUICDM4	R	This is a convulsive force driven micromirror with will be used for CMC demo.
1 Institution(s)			**5 Circuit(s)**		

MEMSCAP 3.0 µm SOIMUMPS

M03S10_1
Technology: MEMSCAP 3.0 µm SOIMUMPS SOIMUMPS
Starting date: 19 January 2010
Delivery of chips: 06 April 2010

Institution	Town	Country	Top Cell	E R I	Function
CMC/Queen's University	Kingston	CA	IMOTRAAA	R	Design a robotic workstation with application to microsurgery.
CMC/Queen's University	Kingston	CA	IMOTRBBB	R	Design of robotic workstation with application to microsurgery.
CMC/Queen's University	Kingston	CA	IMOTRHCD	R	design of microscale components for parallel microassembly process.
1 Institution(s)			**3 Circuit(s)**		

M03S10_2
Technology: MEMSCAP 3.0 µm SOIMUMPS SOIMUMPS
Starting date: 20 April 2010
Delivery of chips: 30 June 2010

Institution	Town	Country	Top Cell	E R I	Function
CMC/Queen's University	Kingston	CA	IMOBCES2	R	The target application deals with a high sensitive capacitive micro-accelerometer, to be integrated iin an adaptive inertial sensor cluster for automotive (path-prediction) and biomedical-applications (non-invasive surgery). The accelerometer we are designing will be integrated with a gyroscope (other graduate student is working on the design of the gyroscope) to form an inertial sensor cluster. For this cluster two of the accelerometers will be used. The cluster will be adaptively controlled by means of FPGA implementation of feedback control loop.
CMC/Queen's University	Kingston	CA	IMODTEW3	R	EW3 (EarthWorm 3) this chip will further develop the earthworm inspired micro-motors investigated on IMUDTEW1 and IMUDTEW2. These next generation motors will be investigated using the SOI MUMPs process due to the higher structure heights available. Friction is an integral part of the locomotion of many small organisms and at Dalhousie we have used these principles for MEMS devices. We have begun investigating earthworm inspired peristaltic motion that uses a squeezing type of motion to propel a micro-device. EW3 focuses on motots that require little-to-no post-processing for their operation.
CMC/Queen's University	Kingston	CA	IMOICDM4	R	This chip contains exemple devices for CMC demo use and test structures with various DRC vialation to check the related failure result. Later it will be used to assemble a document for all CMC clients as reference for their own design.
CMC/Queen's University	Kingston	CA	IMOICIZ4	R	The design includes : - Structure to deduce the intrinsic stress present in the silicon layer as well its Young Modulus. - Bistable switch. - Resonant beams. - Comb resonators.
CMC/Queen's University	Kingston	CA	IMOSFBB3	R	With this design, we want to see the effect of coupling damping on the coupled resonators sensitivity. In our design we eliminated all sources of damping and coupling damping is the most important damping source. Theoretically the sensitivity of this method is high and this design investigates a relatively simple gyroscopes based on this method.
CMC/Queen's University	Kingston	CA	IMOWTNIZ	R	This project involves the design of on-chip tunneling measurement units with temperature-based position sensing and sub-nanometer stability. The objective is to measure tunneling currents using sufficienty robust MEMS actuators.
CMC/Queen's University	Kingston	CA	IMOWTRF2	R	This project will develop a fully integrated silicon-based MEMS device that leverages the frequency selective properties of acoustic band gap crystals, which provide a new paradigm for the design of novel microwave acoustic MEMS technologies. The primary objective of the project is to integrate MEMS electrostatic transducers, for the excitation and sensing of electic waves, with silicon-plate acoustic band gap crystals. Fixed electrodes are utilized in the electrostatic wave transducers.
1 Institution(s)			**7 Circuit(s)**		

M03S10_3
Technology: MEMSCAP 3.0 µm SOIMUMPS SOIMUMPS
Starting date: 20 July 2010
Delivery of chips: 01 October 2010

Institution	Town	Country	Top Cell	E R I	Function
CMC/Queen's University	Kingston	CA	IMOTRHCE	R	In this research, the main objective is to improve the throughput and the productivity of the micro-assembly process through the parallel approach. In this approach, parallel microgrippers are installed on an in-house micromanipulator to grasp and assemble multiple micro-parts simultaneously. The parallel microgrippers and the microparts in this work are designed on the basis of the manufactured capability of the SOIMUMPs process.
CMC/Queen's University	Kingston	CA	IMOWTNIZ	R	The project involves the design of on-chip tunneling measurement units with temperature-based position sensing and sub-nanometer stability. The objective is

					to measure tunneling currents using sufficiently robust MEMS actuators.
CMC/Queen's University	Kingston	CA	IMOWTNS2	R	Scanning Probe Microscope test devices.
1 Institution(s)			**3 Circuit(s)**		

MEMSCAP 8.0 µm MetalMUMPS

M08M10_1
Technology: MEMSCAP 8.0 µm MetalMUMPS MetalMUMPS
Starting date: 19 March 2010
Delivery of chips: 30 June 2010

Institution	Town	Country	Top Cell	E R I	Function
CMC/Queen's University	Kingston	CA	IMMWTMBK	R	The proposed devices will have optimized RF performance and low power consumption that will meet the requirements of COM DEV for the first time. Power consumption with excellent RF performance is the main objective to any system that is targeting aerospace and space industry.
1 Institution(s)			**1 Circuit(s)**		

M08M10_2
Technology: MEMSCAP 8.0 µm MetalMUMPS MetalMUMPS
Starting date: 14 September 2010
Delivery of chips: 07 January 2011

Institution	Town	Country	Top Cell	E R I	Function
CMC/Queen's University	Kingston	CA	IMMWTMBK	R	RF MEMS switches and varactors.
Ghulam Ishaq Khan Institute of Engineering Sciences and Technology	Topi	PK	inertial_sensors	R	Initial sensors used for educational purposes by Master and Phd students.
2 Institution(s)			**2 Circuit(s)**		

B.2 - Turnaround time

In 2010 the average turnaround time, from the closing date of the run to the delivery of packaged chips was:

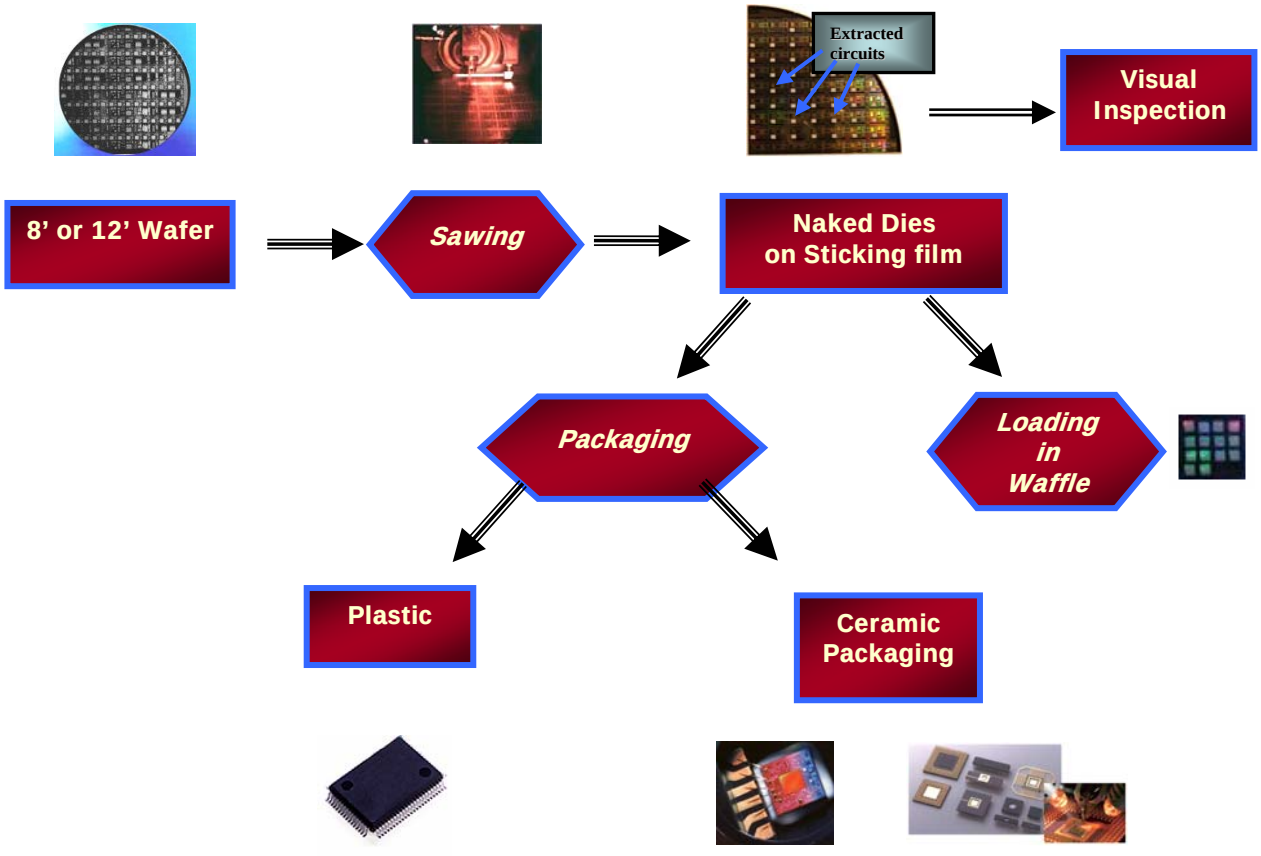
Foundry	Technology	Nb of weeks
austriamicrosystems	0.35 CMOS	12
austriamicrosystems	0.35 SiGe BiCMOS	13
austriamicrosystems	0.35 CMOS-RF	10
austriamicrosystems	0.35 HV-CMOS	11
STMicroelectronics	130 nm CMOS	19
STMicroelectronics	130 nm SiGe	17
STMicroelectronics	65 nm CMOS	22
STMicroelectronics	65 nm SOI	17
MEMSCAP	PolyMUMPS	13
MEMSCAP	MetalMUMPS	16
MEMSCAP	SOIMUMPS	11

The appendix 10 lists the turnaround time for each run.

C – Packaging service

CMP offers a complete assembly service based on a wide range of ceramic and plastic packages for prototyping and low volume production (see also http://cmp.imag.fr/products/packaging)

C.1 - Packaging process flow for MPW runs



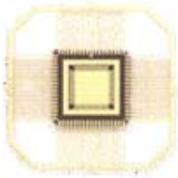
The turnaround time of these overall operations is 1 to 2 weeks

C.2 – Packages

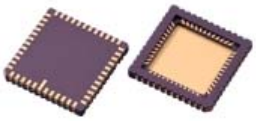
- **Ceramic packages**

DIL
(Dual in Line)

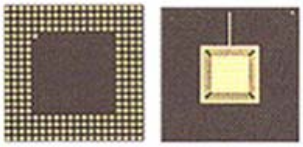
CQFP
(CerQuad Flat Pack)



CLCC - JLCC
(C Leaded Chip Carrier)
(J Leaded Chip Carrier)



PGA
(Pin Grid Array)



SOIC
(Small Outline)

- **Plastic Packages**

1. ***Standard***

PLCC
(Plastic Leaded Chip Carrier)

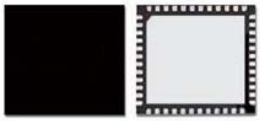
QFP / TQFP
(Quad Flat Package)

SOIC
(Small Outline)

SSOP / TSSOP
(Small Shrink Outline Package)

2. ***Leadless***

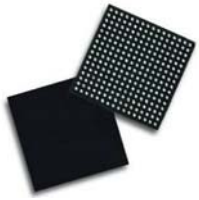
QFN
(Quad Flat No leads)



3. ***Ball Grid Array (BGA)***

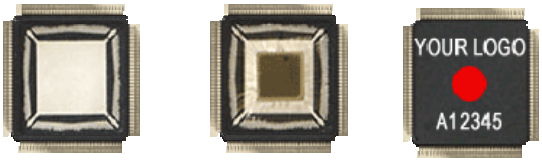
PBGA
(Plastic Ball Grid Array)

fpBGA
(fine pitch Ball Grid Array)



- **<u>Plastic Packages</u>: open cavity**

QFP , QFN , PLCC
SOIC , TSSOP . . .



C.3 – Specific packaging

- Optical resin
- Hybrid
- Chip On Board (COB)
- Flip-Chip: available at die level, up to 32 IO
- Thermal solutions
- Metallic package
- Chip Scale Package (CSP)
- Microsystems packaging

C.4 – Analysis and Quality

- Naked dies are visually inspected (before the packaging) in accordance with MIL-STD 883 (Method 2010 Cond. A or B)
- Visual inspection for ceramic bonding checking
- X-ray test on few samples for plastic bonding checking

C.5 – Additional services

- Additional packaging from previous runs
- A conditioning service is available for wafers and naked dies Storage is done in vacuum or nitrogen atmosphere and may be useful in case of production to be spread out over a period of time.
- Wafer and die back lapping

C.6 - Customer inputs

<u>From CMP web site, the designer will find:</u>

1. Blank package cavity diagram (plastic on request) allowing to draw bonding diagram.
2. Package data sheet : mechanical map

<u>Package choice:</u>

- The designer specifies the package type with the cavity, body size …
- Otherwise the designer specifies the package type and CMP will choose the most suitable package with the most appropriate cavity size according to the size of the circuit.

<u>Bonding Diagram:</u>

- The designer can draw the bonding diagram with CAD tools and include it with his design in Cadence, Mentor… database (GDSII file) or on PC tools such as PowerPoint.

or

- CMP can make the most suitable bonding diagram which will be communicated to the designer for approval.

General assembly rules and common errors are available on the web site.

D – Analysis of the participation

In 2010 a total of 354 circuits were fabricated for 122 organizations (Universities, Research Laboratories and Industrial Companies) all over the world (23 countries). See the list of participants in Appendix 2. Hereafter are the technologies used in 2010:

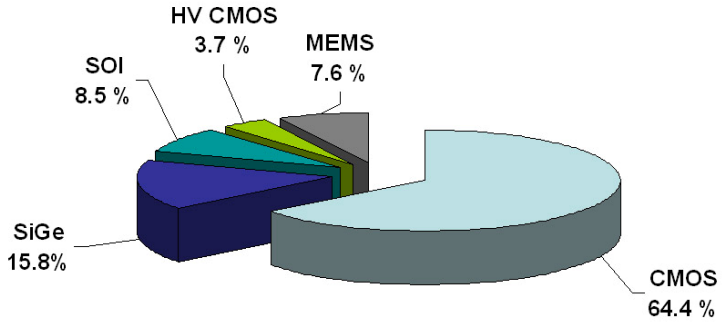
For Integrated Circuits:

- 0.35 µ C35B4C3 CMOS DLP/4LM austriamicrosystems

- 0.35 µ C35B4O1 CMOS-Opto DLP/4LM austriamicrosystems
- 0.35 µ H35B4D3 CMOS DLP/4LM High Voltage austriamicrosystems
- 0.35 µ C35B4E3 CMOS DLP/4LM EEPROM / Flash austriamicrosystems
- 0.35 µ S35D4M5 SiGe BiCMOS DLP/4LM austriamicrosystems
- 130 nm HCMOS9 CMOS 6LM STMicroelectronics
- 65 nm CMOS065 CMOS 7LM STMicroelectronics
- 40 nm CMOS045 CMOS 7LM STMicroelectronics
- 65 nm CMOS065-SOI SOI 6LM STMicroelectronics
- 130 nm HCMOS9-SOI SOI 6LM STMicroelectronics
- 130 nm BiCMOS7RF SiGe BiCMOS STMicroelectronics

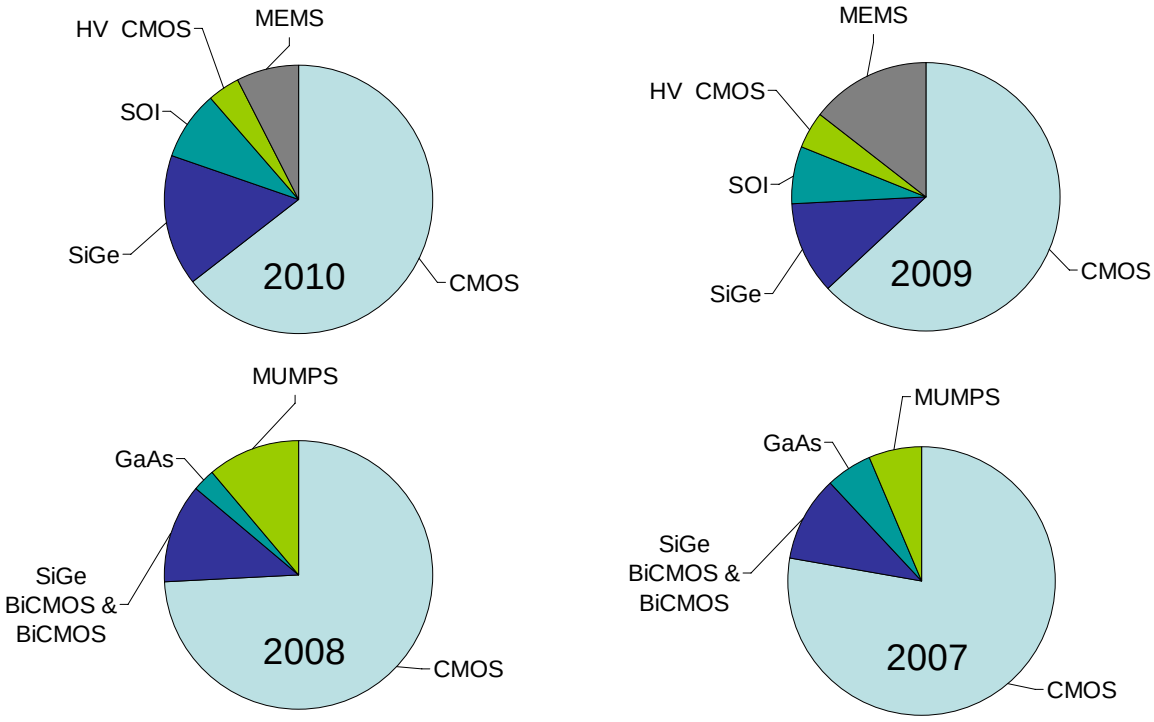
For Micro Electro Mechanical Systems:
- 0.35 µ CMOS bulk micromachining CMP/austriamicrosystems
- Multi-User MEMS Process PolyMUMPS from MEMSCAP
- Multi-User MEMS Process MetalMUMPS from MEMSCAP
- Multi-User MEMS Process SOIMUMPS from MEMSCAP
- SUMMiT V Process from SANDIA

D.1 - Distribution of circuits per technology and evolution



Distribution of circuits per technology in 2010

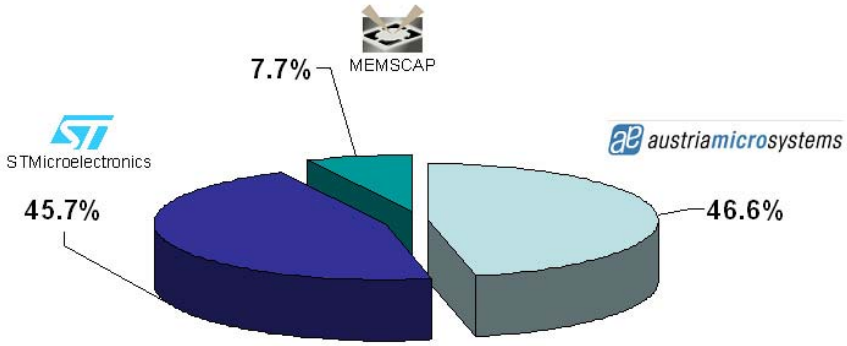
In 2010 the part of CMOS (with SOI and High Voltage) is 76.6% of the total. CMOS plus BiCMOS represent 92.4% of the total and MEMS 7.6%.



Evolution of circuits per technology from 2007 to 2010

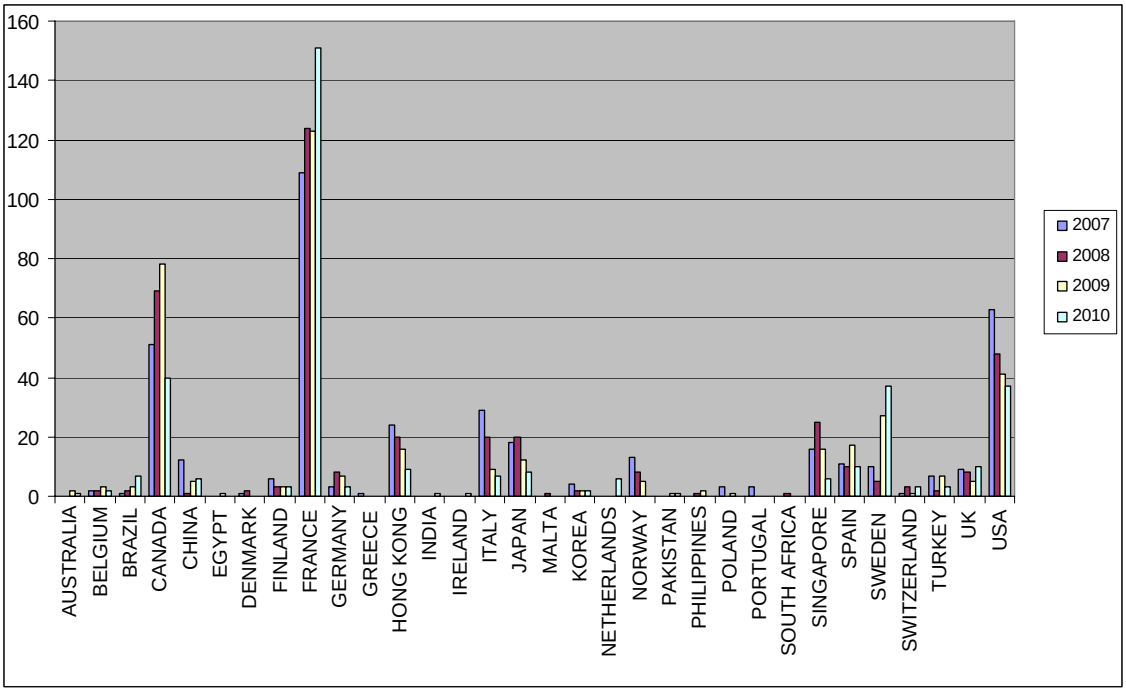
For the last four years the part of CMOS is stable and represents more than 70% of the circuits. The remaining part is shared between BiCMOS, MUMPS and GaAs.

D.2 - Distribution of circuits per foundry

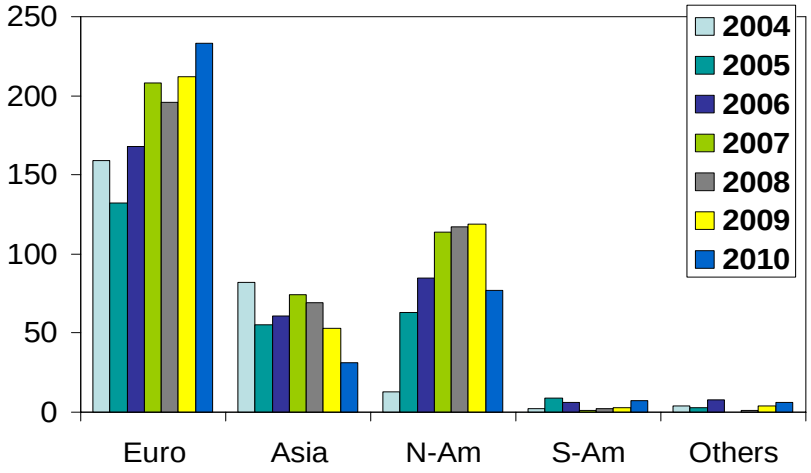


Distribution of circuits per foundry in 2010

D.3 - Distribution of circuits per country and geographical area

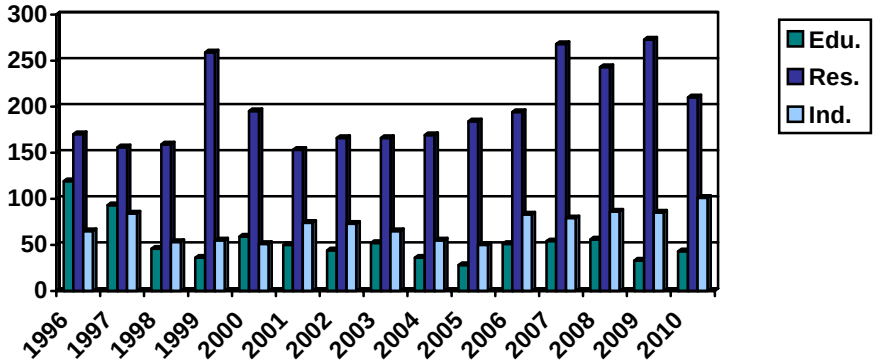


Distribution of circuits per country in 2007, 2008, 2009 and 2010



Distribution of circuits per geographical area and evolution from 2004 to 2010

D.4 - Distribution of circuits per utilization



Distribution of circuits per utilization from 1996 to 2010

Circuits for education, France

3 circuits have been submitted in 2010. The Appendix 6 shows the evolution since 1991.

Circuits for research

Circuits for research represent 210 circuits (60%) coming from 22 countries.

Circuits for industry

In 2010, 101 industrial circuits, 66 from France and 35 from foreign countries, were fabricated for 25 industrial companies or national research laboratories (see the list in Appendix 4). This level of industrial participation represents 28% of the total number of circuits. They were manufactured for prototyping or low volume production: 80 low volume circuits for 31 Institutions, from thirty pieces to thousands of pieces. See in Appendix 5 the list of low volume circuits.

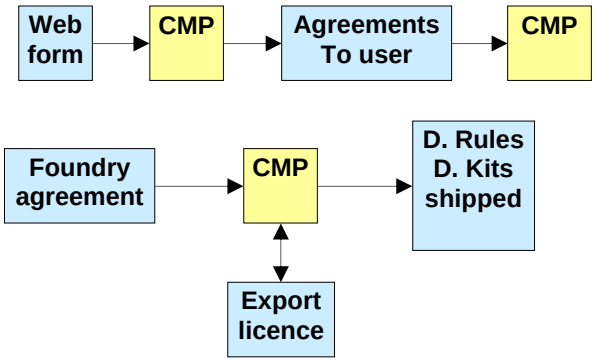
New Institutions

In 2010, 25 Institutions (out of 109 all in all) participated for the first time as listed in the Appendix 3. All the Institution having submitted circuits from 1981 are listed in Appendix 7.

E – Design kits management

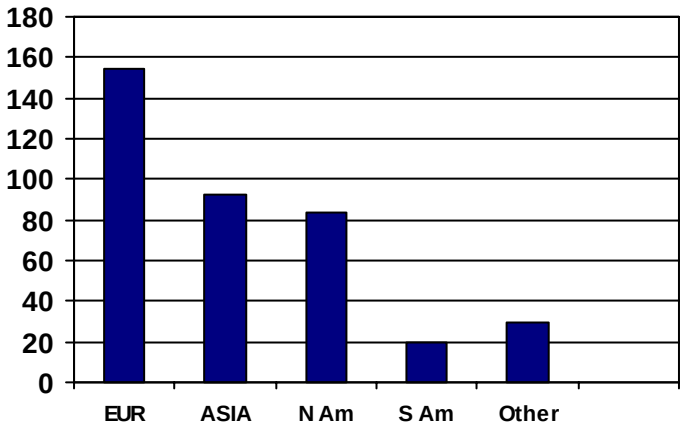
CMP distributes the design rules for each technology and the standard cell libraries for each specific software tool (design kits). CMP handles about 33 different design kits (corresponding to different technologies and different CAD tools), which are sent to customers upon signature of a Confidentiality and License Agreement. Almost all of them are sent free of charge. About 1060 customers, (academic centres and industrial companies) from 66 countries have already signed agreements and received design kits. The Appendix 9 presents the list of the design kits.

The following figures present the procedure to get design kits.

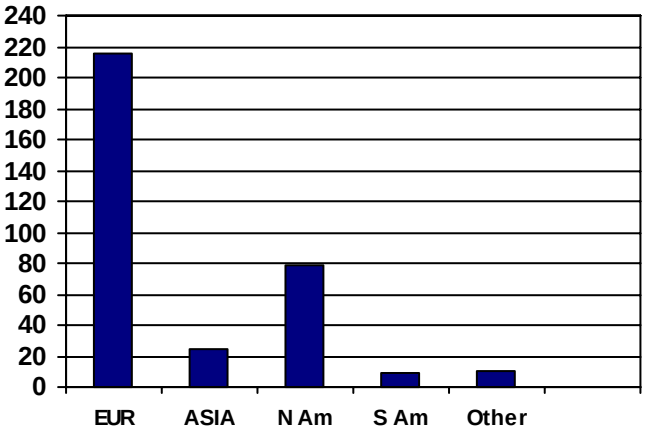


Procedure to get design kit

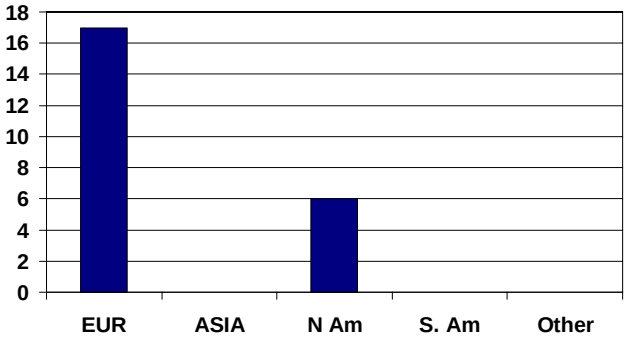
The figures below show the distribution of design kits per foundry and zone, in total number of Institutions.



Austriamicrosystems (1991-2010)

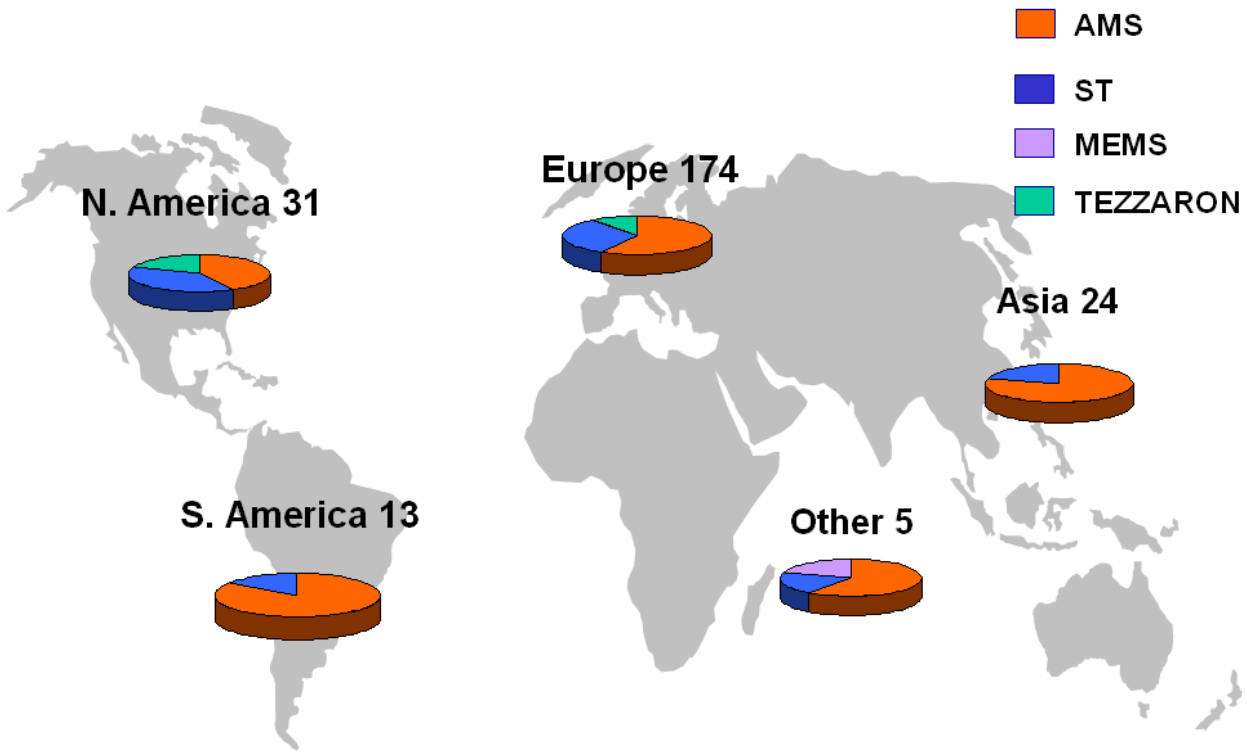


STMicroelectronics (2006-2010)



Tezzaron (2010)

Globally the number of Institutions which received design kits are:
- 380 Institutions for austriamicrosystems.
- 30 new Institutions for STMicroelectronics with a total of 480 institutions since 2002.



Design kits distribution in 2010

- Globally in 2010, 33.78% of the Institutions applied for austriamicrosystems, 66.22% for ST.
- CMP customers mainly come from Europe (70.44%), North America (12.55%) and Asia (9.72%). Other customers come from South America, Arabic countries and Australia.

F – Runs scheduled in 2010:

austriamicrosystems	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
C35B4C3 0.35 µm CMOS		14			30		18		5		2	12
C35B4O1 0.35 µm CMOS Opto		14			30		18		5		2	12
C35B4M3 0.35 µm CMOS Thick M4		25				3			2		18	
H35B4D3 0.35 µm HV-CMOS		11		22				5			4	
S35D4M5 0.35 µm SiGe		25				3			2		18	
STMicroelectronics	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
CMOS040LP 40 nm CMOS		16	23			22				26		
CMOS065 65 nm CMOS			28			10				17		
HCMOS9GP 130 nm CMOS	12			27			5			5		
BiCMOS9MW 130 nm SiGe	12			27			5			5		
HCMOS9-SOI 130 nm SOI	12			27			5			5		
MEMSCAP	**Jan**	**Feb**	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**
MUMPS 2.0 µm polyMUMPS	4			5			5			4		
MUMPS 3.0 µm SOIMUMPS	18			19			19			18		
MUMPS 8.0 µm metalMUMPS			8						13			