

XIII - CONCLUSIONS

Several conclusions are addressed in the following, according to 2 broad lines:

- more Moore
- more than Moore

and 2 considerations:

- going global
- being excellent

A – More Moore

It has been recognized that Students, Researchers and SME designers must be provided with the possibility to have their circuits fabricated. From its inception in 1981, CMP has been successfully pursuing this goal and experiencing a very significant growth to reach and to keep its present level. The success is partly due to the basic principles which have been governing the choices of the Service: use of industrial and advanced process lines. Advanced processes are more and more necessary because of the need for very skilled designers and because CAD industrial software is more widely available to Universities (instead of University CAD software). Since new versions of CAD software are targeted to industrial use, there is no choice but to use advanced processes. Industry makes also more and more use of the Service. During the 80s, the CMP processes were not very advanced, but they approached more and more industry state of the art during the 90s, because of CAD software reasons and because of the increasing industry use of CMP. Since then, CMP has been always offering state of the art processes.

More specifically the following table summarizes the evolution in silicon fabrication and participation during the nineteen last years.

YEAR	NB OF CIRCUITS	NB OF INSTITUTIONS	TECHNOLOGIES
1992	114	38	ES2 1.5 μ , 1.2 μ CMOS TCS Bip AMS 2 μ 2M2P, 1.2 2M2P more integration ↓
1993	197	55	ES2 1.5 μ , 1.2 μ , 1.0 μ CMOS TCS Bip AMS 2 μ 2M2P, 1.2 2M2P, 1.2 μ 2M 2P BiCMOS TCS 0.8 μ Dig. GaAs more integration ↓
1994	251	75	ES2 1.5 μ , 1.2 μ , 1.0 μ , 0.7 μ CMOS TCS Bip AMS 1.2 μ 2M2P, 1.2 μ 2M 2P BiCMOS 0.8 μ 2M1P VSC 0.6 μ Dig. GaAs STM 0.5 μ TLM more integration ↓
1995	298	94	ES2 1.2 μ , 1.0 μ , 0.7 μ CMOS TCS Bip AMS 1.2 μ 2M2P, 1.2 μ 2M 2P BiCMOS 0.8 μ 2M2P, 0.8 μ 2M2P BiCMOS VSC 0.6 μ Dig. GaAs PML 0.2 μ HEMT GaAs more integration ↓
1996	354	107	ES2 1.2 μ , 1.0 μ , 0.7 μ CMOS TCS Bip AMS 1.2 μ 2M2P, 1.2 μ 2M 2P BiCMOS 0.8 μ 2M2P, 0.8 μ 2M2P BiCMOS VSC 0.6 μ Dig. GaAs PML 0.2 μ HEMT GaAs more integration ↓
1997	333	112	ES2 1.0 μ , 0.7 μ CMOS AMS 1.2 μ 2M2P, 1.2 μ 2M 2P BiCMOS 0.8 μ 2M2P, 0.8 μ 2M2P BiCMOS 0.6 μ 2M 2P VSC 0.6 μ Dig. GaAs PML 0.2 μ HEMT GaAs more integration ↓

1998	259	94	<p>ES2 0.7 μ CMOS AMS 1.2 μ 2M2P, 1.2 μ 2M 2P BiCMOS 0.8 μ 2M2P, 0.8 μ 2M2P BiCMOS 0.6 μ 2M 2P ST 0.25 μ 6M CMOS VSC 0.5 μ Dig. GaAs PML 0.2 μ HEMT GaAs MCNC MUMPs surface micromachining</p> <p style="text-align: right;">↓ more integration</p>
1999	348	100	<p>AMS 1.2 μ , .8 μ , 0.6 μ , 0.35μ CMOS 1.2 μ , 0.8 μ BiCMOS 0.8 μ HBT CMOS (SiGe) ST 0.25 μ CMOS PML 0.2 μ HEMT GaAs CRONOS MUMPs surface micromachining</p> <p style="text-align: right;">↓ more integration</p>
2000	305	103	<p>AMS 1.2 μ , 0.8 μ , 0.6 μ , 0.35μ CMOS 0.8 μ BiCMOS 0.8 μ HBT CMOS (SiGe) ST 0.25 μ , 0.18μ CMOS OMMIC 0.2 μ HEMT GaAs CRONOS MUMPs surface micromachining</p> <p style="text-align: right;">↓ more integration</p>
2001	277	97	<p>austriamicrosystems 0.8 μ , 0.6 μ , 0.35μ CMOS 0.8 μ BiCMOS 0.8 μ HBT CMOS (SiGe) STMic. 0.25 μ , 0.18μ CMOS Peregrine 0.5μ SOI/SOS CMOS OMMIC 0.2 μ HEMT GaAs CRONOS MUMPs surface micromachining</p> <p style="text-align: right;">↓ more integration</p>
2002	282	89	<p>austriamicrosystems 0.8 μ , 0.6 μ , 0.35μ CMOS 0.8 μ , 0.35μ BiCMOS 0.8 μ HBT CMOS (SiGe) ST. 0.18 μ , 0.12μ CMOS 0.35 μ HBT CMOS (SiGe) Peregrine 0.5μ SOI/SOS CMOS OMMIC 0.2 μ HEMT GaAs CRONOS MUMPs surface micromachining</p> <p style="text-align: right;">↓ more integration</p>
2003	283	85	<p>austriamicrosystems 0.8 μ , 0.6 μ , 0.35μ CMOS 0.8 μ , 0.35μ BiCMOS 0.8 μ HBT CMOS (SiGe) ST 0.18 μ , 0.12μ CMOS 0.35 μ SiGe BiCMOS Peregrine 0.5μ SOI/SOS CMOS OMMIC 0.2 μ HEMT GaAs MEMSCAP PolyMUMPs, SOIMUMPs</p> <p style="text-align: right;">↓ more integration</p>
2004	260	86	<p>austriamicrosystems 0.8 μ , 0.6 μ , 0.35μ CMOS 0.35μ CMOS-opto, 0.35μ CMOS-RF 0.8 μ BiCMOS 0.35μ SiGe BiCMOS ST 0.18 μ , 0.12μ CMOS 0.35 μ SiGe BiCMOS OMMIC 0.2 μ HEMT GaAs MEMSCAP PolyMUMPs</p> <p style="text-align: right;">↓ more integration</p>

2005	262	94	austriamicrosystems 0.6 μ , 0.35μ CMOS 0.35μ CMOS-opto, 0.8 μ BiCMOS 0.35μ SiGe BiCMOS ST 0.18 μ, 0.12μ, 90 nmCMOS 0.35 μ SiGe BiCMOS 0.25 μ SiGe:C BiCMOS OMMIC 0.2 μ HEMT GaAs MEMSCAP PolyMUMPs ↓ more integration
2006	329	93	austriamicrosystems 0.6 μ , 0.35μ CMOS 0.35μ CMOS-opto, CMOS HV, CMOS RF 0.35μ SiGe BiCMOS ST 0.12μCMOS, 90 nmCMOS, 65 nm CMOS 0.35 μ SiGe BiCMOS 0.25 μ SiGe:C BiCMOS CSMC 0.6 μ CMOS OMMIC 0.2 μ HEMT GaAs MEMSCAP PolyMUMPs, SOIMUMPS, MetalMUMPS↓ more integration
2007	401	105	austriamicrosystems 0.35μ CMOS 0.35μ CMOS-opto, CMOS HV, CMOS RF 0.35μ SiGe , 0.35μ HV EEPROM ST 0.12μCMOS, 90 nmCMOS, 65 nm CMOS 0.35 μ SiGe BiCMOS 0.25 μ SiGe:C BiCMOS CSMC 0.6 μ CMOS OMMIC 0.2 μ HEMT GaAs MEMSCAP PolyMUMPs, SOIMUMPS, MetalMUMPS↓ CSMC 0.6 μ CMOS Bulkmicromachining ↓ more integration
2008	375	89	austriamicrosystems 0.35μ CMOS 0.35μ CMOS-opto, CMOS HV, CMOS HV EEPROM, CMOS RF 0.35μ SiGe BiCMOS 0.35μ CMOS bulk micromachining ST CMOS: 130 nm, 90 nm, 65 nm, 45 nm SOI: 130 nm, 65 nm 0.25 μ SiGe:C BiCMOS OMMIC 0.2 μ HEMT GaAs 0.2μ HEMT Bulk micromachining MEMSCAP PolyMUMPs, SOIMUMPS, MetalMUMPS ↓ SANDIA SUMMiT V ↓ more integration
2009	391	104	austriamicrosystems 0.35μ CMOS 0.35μ CMOS-opto, CMOS HV, CMOS HV EEPROM, CMOS RF 0.35μ SiGe BiCMOS 0.35μ CMOS bulk micromachining ST CMOS: 130 nm, 90 nm, 65 nm, 40 nm SOI: 130 nm, 65 nm MEMSCAP PolyMUMPs, SOIMUMPS, MetalMUMPS ↓ SANDIA SUMMiT V ↓ more integration

2010	354	122	austriamicrosystems 0.35μ CMOS/CMOS-opto, CMOS HV, CMOS HV EEPROM 0.35μ SiGe BiCMOS 0.35μ CMOS bulk micromachining ST CMOS: 130 nm, 65 nm, 40 nm SOI: 130 nm, 65 nm SiGe BiCMOS: 130nm TEZZARON/ GLOBALFOUNDRIES 2 Tiers 3D-IC/130nm CMOS CEA-LETI 20 nm FDSOI MEMSCAP PolyMUMPs, SOIMUMPS, MetalMUMPS SANDIA SUMMIT V <div style="text-align: right;">↓ more integration</div>
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Key issues in 2010 are:

- ▶ large portfolio of technologies down to 20nm
- ▶ introduction of a 3D process in cooperation with CMC in Canada and MOSIS in the USA

But cost and acceptance are slowing down the use of ever advanced processes. Practical difficulties are popping up like power density, temperature, variability, leakage power, analog design, etc. The costs are rising high if circuits are not manufactured in very large volumes. A way to overcome the cost issue while keeping costs reasonable is to go for larger die sizes on current-generation geometrics. But anyway fundamental limits coming from thermodynamics, quantum mechanics, electromagnetics, ... will set show stoppers sooner or later.

B - More than Moore

The quest for always larger densities may also be satisfied with 3D integration, possibly not including very advanced process dies for cost reasons. System in package integration (SiP) allows heterogeneous integration, like sensors, electronics, etc. opposed to systems on chip (SoC) in which all parts are manufactured on the same process, which is not always optimal.

3D processes using TSVs (Through Silicon Vias) allow to go one step further: interconnections are shorter, hence leading to power savings and better performance, there are less I/Os so less power is consumed. Heterogeneous integration is also possible as for SiP. There are still concerns to be addressed like thermal issues (increased density may lead to hot spots, electromigration,...), power (no power savings if current-generation geometrics are used), CAD software. CMP has introduced a 3D process using TSVs in 2010.

A step further may be required for some applications where the substrate is required to be flexible, like for many BioMed applications. Organic electronics allow 3D integration as well, for a cheap cost, for large areas, for heterogeneous integration. Biocompatibility is also a plus for BioMed applications. B. KAMINSKA et al. have introduced a good example of such systems. A multilayer polymer microsensor system allows skin tissue conformity since the substrate can bend up to 30°. It includes various sensors, signal conditioning, processing, RF communication, powering from disposable or rechargeable batteries. The prototype includes electrodes for ECG and a MEMS accelerometer for body positioning calculation.

It is also recognized that complementary developments must be addressed, in order to address more diversified needs. With this respect, CMP has been a pioneer in being the first service in the world to offer MEMS processes as early as 1995. Going further, more than mechanics-electronics is to be addressed like photonics, optics, fluidics, etc. CMP will be actively promoting these developments in the future (see Appendices 18 and 19).

C - Going global

The cooperation between service organizations has already been mentioned.

On the side of the users of CMP and of other similar services, the design way is also going more and more global in the sense that more and more IP blocks may come from various sources. This is due to the ever increasing complexity of designs, including parts coming from various teams, countries, companies, etc. An initiative is being developed to go this way: the Global Education for Microelectronic Systems (GEMS).

D - Being excellent

Globalization also requires to be excellent in order to stay ahead of others. This is important at the time of global markets, when every country or continent is a high cost country or continent to another one. Some countries or continents that were said to be "low-cost" countries or continents a few years ago already experience that other countries or continents are coming to the picture with lower costs, forcing them to outsource their own outsourcing. The way to combat that is to stay ahead of the others. The way to stay ahead is to educate and research using top level electronic processes available from top level services like CMP.

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