

G - Survey of major foreign national MPC services

The following reflects the most recent available information. More information on most of these services can be found in the following paper: COURTOIS B, "Infrastructures for education and research: from national initiatives to worldwide development", invited paper at Festkolloquium Zukunftstrends in der Mikroelektronik Anlass: von 60. Geburtstag Professor Manfred Glesner, Darmstadt, Germany, August 29, 2003.

Canada

CMC Microsystems enables and supports the creation and application of micro- and nano-system knowledge by providing a national infrastructure for research excellence and a path to commercialization of related devices, components and integrated microsystems. CMC manages two major projects valued at over \$170 million (2010-2015) enabling delivery of tools and technologies to Canada's National Design Network. This Network involves multi-disciplinary research often leading to complex prototype microsystems and is dependent on the interactions between many individuals and organizations. For almost 30 years CMC has delivered innovative and cost-effective services to a growing community of microsystems researchers that presently connects 850 faculty members and their 2,000 post-graduate students in 47 post-secondary institutes and indirectly more than 400 companies.

In 2011, the Embedded Systems Canada project started to take shape. Preliminary deliveries were of CAD tools for which there are plans for significant growth. A real-time embedded software lab was constructed. In general, the infrastructure will consist of research labs in more than 35 universities connected by secure links to a management hub, with operations based at CMC. Researchers will use a range of multi-technology design environments, development systems, microsystem rapid prototyping and characterization labs, as well as support and training services.

An overview of CMC-supported products and services for R&D is available at <http://www.cmc.ca/WhatWeOffer/Documents/ProductCatalog.aspx>; including:

- Providing access to and supporting environments for the design of digital, analog, RF and mixed-signal integrated circuits; MEMS, microfluidic and photonic/optoelectronic devices; embedded systems. Environments include industry-relevant CAD tools, design kits, IP and methodology.
- Coordinating microsystem fabrication services including design-rule check and packaging services (over 360 designs managed in 2011) targeting a portfolio of technologies.
 - TSMC 65nm CMOS through MOSIS
 - TSMC 90nm CMOS through MOSIS
 - TSMC 0.18µm CMOS through MOSIS
 - TSMC 0.35µm CMOS through MOSIS
 - IBM 0.13µm CMOS through MOSIS
 - AMS 0.35µm CMOS through CMP
 - 0.8-micron GaN, CPFC, Ottawa
 - 0.5-micron GaN, CPFC, Ottawa
 - LTCC (Low Temperature Co-fired Ceramics), IMST GmbH, Germany
 - Tezzaron 3D-IC on 0.13 µm CMOS, CMC Microsystems in collaboration with CMP and MOSIS
 - 2.5 GHz Bipolar Linear Array training technology, by special arrangement
 - 0.8µm CMOS, high/medium/standard voltages, Teledyne Dalsa Semiconductor
 - MEMSCAP PolyMUMPs
 - MEMSCAP MetalMUMPs
 - MEMSCAP SOIMUMPs
 - Tronics MEMSOI
 - UW-MEMS, CIRFE Lab, University of Waterloo
 - Sonosit (glass-based microfluidic process with metallization), Micronit
 - OFEX, (silicon nitride planar optical waveguides with microfluidic channels), LioniX
 - III-V Epitaxy on InP and GaAs substrates, CPFC, Ottawa
 - III-V Epitaxy on GaAs, Landmark Optoelectronics Corporation
 - III-V InP process, CRN2, Université de Sherbrooke
 - III-V InP, GaAs and SOI processes, CPFC, Ottawa
 - ePIXfab Silicon-on-Insulator through IMEC
 - NanoSOI, CMC Microsystems in cooperation with INO and Applied Nanotools

- Maintaining a Micro-Nano Technologies web portal that provides detailed information about fabrication facilities, equipment and processes based at university labs in Canada; and providing financial assistance for laboratory use by Canadian researchers.
- Enabling clients to measure the characteristics of their implemented designs.
 - Providing package services including models and fixturing solutions.
 - Providing short-term loans of test equipment, including unique customized items, such as a portable “Photonics Chip-on-Carrier Test Stage” for microfluidics research in the field.
 - Managing the National Microelectronics and Photonics Testing Collaboratory’s four laboratories (digital, RF, analog mixed-signal microelectronic test labs and a photonics test lab).
- Supporting prototyping environments that enable interconnection of electronic, photonic, mechanical and fluidic technologies, embedded software, and wireless interfaces:
 - Carrier platform for microfluidics
 - Compact wireless development platform
 - MEMS-FPGA development platform
 - BEE3 FPGA development system
 - Embedded software development flows supported on all platforms
 - Offering special packaging and assembly services to assist development of integrated microsystems. Examples include: stacked-die, die-in-package, multi-die-in-package, die-on-board, or multi-die-on-board assembly or 3-D stacking using wire bonding or flip-chip; hermetic packaging and encapsulation; laser-assisted cleaving; parylene coating.
- Providing instruction (training, tutorials) for supported CAD tools and related fabrication technologies; workshops on GaN, wafer post-processing, and microfluidics/nanofluidics research; a webinar series about design-for-testability in 3D-IC design.
- Helping researchers benefit from shared experiences by soliciting and distributing *Microsystem Integration Application Notes* (25-35 published yearly through CMC) with topics such as:
 - Simulating Air-Bridges of CPFC GaN MMIC in Momentum
 - Adding Package Libraries to a Cadence Allegro PCB Design XL Project
 - Force Transducer Design for Measuring Neck Muscular Efforts in Paediatrics
 - CMC Compact Wireless Platform for Animat Applications
 - Embedded Software Development and Power Monitoring for the CMC Compact Wireless Platform

CMC organizes a national symposium on microsystems research and development and other supporting workshops annually. The theme of the 2011 symposium was “Energy Matters”. Topical notices on technological development are issued electronically via monthly bulletins. These bulletins and detailed information on CMC’s operations and plans are at: <http://www.cmc.ca>.

China

Founded in 2000 by Science and Technology Commission of Shanghai Municipality, Shanghai IC Technology & Industry Promotion Center (ICC) is dedicated in promoting Shanghai and all China IC Design industry to realize durative rapid development. ICC established the public service platform open to all IC design enterprises, universities and research institutes, providing full services to improve design quality and lower the cost. The services ICC provides include Multi-Project Wafer service, SoC design platform, testing service, training and evaluation, information service, etc. In addition, ICC is a vice council director of China Semiconductor Industry Association IC Design Branch, a vice council director of Shanghai IC Industry Association, and the director of Shanghai IC Industry Association IC Design Branch, a vice council director of Shanghai IC Industry Association. From 1996 to 2000, Shanghai MPW Service (SMS), operated by Fudan University, was mainly open to academic users, with totally 116 designs fabricated. From 2001, ICC began to operate SMS, expanded the service to industrial sectors and became the China National MPW Center. Totally 2422 designs from more than 310 design houses, universities and research institutes were prototyped on MPW runs and low volume production since 2001.

The following technologies were available in SMS in 2011:

- TSMC 65nm CMOS
- TSMC 90nm CMOS
- TSMC 0.13um CMOS
- TSMC 0.18um CMOS
- TSMC 0.25um CMOS
- TSMC 0.35um CMOS
- TSMC 0.35um SiGe

- SMIC 65nm CMOS
- SMIC 90nm CMOS
- SMIC 0.13um CMOS
- SMIC 0.18um CMOS
- SMIC 0.35um EEPROM
- GLOBALFOUNDRIES 65nm CMOS
- GLOBALFOUNDRIES 0.13um CMOS
- GLOBALFOUNDRIES 0.18um CMOS
- GLOBALFOUNDRIES 0.25um CMOS
- GLOBALFOUNDRIES 0.35um CMOS
- HJTC 0.18um CMOS
- HJTC 0.25um CMOS
- GRACE 0.18um CMOS
- GRACE 0.18um eFlash
- GRACE 0.13um CMOS

There are totally 52 runs in the year of 2011. 520 chips from 102 customers were successfully fabricated. Among those, 229 were industrial projects, the remaining 291 were educational and research projects. Prototype and low volume assembly and test service are also offered.

To address the requests of testing, ICC has set up the most advanced testing center in China mainland which can provide testing service, products verification / validation service to IC companies with ultra low costs. ICC cooperates with its partners to provide an SoC design total solution, which covers from system design / verification, IP sourcing, SoC EDA tools, RTL-to-GDSII Services, Testing service, and system / software integration. The SoC platform is to help IC design companies to enter into SoC design era with low risk and low cost. All the functions or services ICC provides are aiming to strengthen the design capability of the design house and academics in China. More information can be found at ICC's web site: <http://www.icc.sh.cn/>

Japan

VLSI Design and Education Center (VDEC), which is located in the University of Tokyo, has been utilized by academic users in Japan since its foundation in May, 1996. As an MPC service center, VDEC aims at improvements of education on VLSI design and supports on VLSI chip fabrication for national universities, public universities, private universities and colleges in Japan. VDEC receives a lot of supports from Japan government, as well as semiconductor industries through STARC (Semiconductor Technology Academic Research Center).

Presently the following technologies are available for chip fabrication service.

- 1-poly 8-metal CMOS 40nm process from Renesas Electronics Corporation
- 1-poly 12-metal CMOS 65nm process from e-Shuttle, Inc.
- 2-poly 2-metal CMOS 1.2μm process from SCG Japan Ltd. (OnSemiconductor Ltd.)
- 1-poly 5-metal CMOS 0.18μm process from Rohm Co. Ltd.
- 1-poly 4-metal SiGe SOI BiCMOS 0.25μm process from Hitachi Ltd.
- 2-poly 3-metal BiCMOS 0.35μm process from NTT Advanced Technology Corporation.
- VDEC-MOSIS Si-Ge BiCMOS 130nm process from IBM
- VDEC-MOSIS CMOS 130nm processes from IBM
- VDEC-MOSIS CMOS 500nm process from OnSemiconductor Ltd.

From the last year, there are two new processes which were added to our chip fabrication service. One is CMOS 40nm process from Renesas Electronics Corporation. We expect that this process will be actively utilized in the filed of very advanced circuit designs in Japanese academia. The other is BiCMOS 0.35μm process provided from NTT Advanced Technology Corporation. This process was introduced to provide the chance to fabricate their circuit idea as LSI chips for opt-electronics and MEMS researchers in Japan. At the same time, we continue the service of CMOS 0.18μm, 1.2μm, and 65nm processes so that VDEC users can choose their suitable process to meet their research purposes.

In the last VDEC fiscal year (2010.4 – 2011.3), we have provided totally 14 chip fabrication runs to our users. 241 professors (i.e. research groups) from 84 universities and colleges participated chip design and fabrication through VDEC. Totally 241 chips on 2180 mm² silicon area were designed and fabricated utilizing VDEC service, and delivered to the usres. VDEC makes contracts with mainstream CAD vendors and

provides 500 to 1000 CAD licenses for each CAD tool to end-users. In the last year, totally about 13,000 CAD software licenses were issued to 300 lab or group users. To provide high-speed access to CAD tool users at different districts, VDEC set up branches in 9 universities in the whole country.

In addition, VDEC holds a super clean room and various facilities including EB writer and FIB writer for researchers in universities. Logic testers, EB prober and FIB modification system are also provided for chip verification service.

Besides, since 2003, some MOSIS chip fabrication technologies, such as IBM CMOS and IBM Si-Ge BiCMOS, have been provided to VDEC users at a lower cost based on a close VDEC-MOSIS cooperative relationship.

The VDEC Designers Forum 2011, which was the 15th of a series of the forum, was held at Tokyo in June, 2011. This forum provided a good chance for VDEC users to exchange their experience on chip designs and tests. Besides, a set of self-teaching material for IC design with popular CAD tools, including text and exercising data, was also developed for users. It can be freely downloaded from VDEC web site.

Korea

IDEC(Integrated Circuit Design Education Center) has taken initiatives to improve the quality of VLSI design education as well as the research environments in Korean universities, since its establishment in 1995. Throughout the last 17 years IDEC intends to (a) build-up and strengthen the infrastructure of VLSI design education; (b) train highly-qualified VLSI system designers; and (c) contribute to Korean semiconductor industries by promoting collaborations between universities and industries.

To accomplish these objectives, IDEC emphasizes

- ① active operation of education systems that keep pace with current demands.
- ② experience-oriented education based on practical training and projects.
- ③ enlargement of education opportunity by sharing networks and high-cost equipment.
- ④ continuous nationwide improvement of university-level education and research environment by means of Working Group activities.
- ⑤ building IC technology information networks.
- ⑥ promoting systemization, standardization, specialization, and upgrade of educational materials.
- ⑦ building systematic and versatile networks for prompt acquisition of information.

Some of the projects that IDEC has supported include providing opportunities to fabricate chips through MPW (Multi-Project Wafer), providing EDA tools for free or at low cost, and holding open lectures. The designers educated by IDEC, who are highly experienced in EDA tool usage and making real chips, will play a significant role in reinforcing the competitiveness of Korean semiconductors and system industries. The aforementioned projects will make it possible to secure superior designers equipped with new technology and the ability to apply it, lighten the burden of investment by corporations in human resource development, accumulate a variety of IPs, and even accelerate technology innovation as a basis of reinforcing national competitiveness in the twenty-first century as a consequence.

IDEC provides MPW services for 68 Working Groups (WGs) in Korea. As of March 2012, a total of 3,135 IC chips have been successfully fabricated through the IDEC MPW program (328 chips during 2011). The technologies provided in 2012 are listed below:

- CMOS 65nm, 1-poly 8-metal, Samsung Electronics
- CMOS 0.13 μ , 1-poly 6-metal, Samsung Electronics
- CMOS 0.35 μ , 2-poly 4-metal, Magnachip/Hynix
- CMOS 0.18 μ , 1-poly 6-metal, Magnachip/Hynix
- CMOS 0.11 μ , 1-poly 6-metal, Dongbu HiTek
- BCDMOS 0.18 μ , 2-poly 4-metal, Dongbu HiTek
- BCDMOS 0.35 μ , 2-poly 4-metal, Dongbu HiTek
- CMOS Image Sensor 0.18 μ , 1-poly 4-metal, TowerJazz
- RFCMOS 0.18 μ , 1-poly 6-metal, TowerJazz
- SiGe BiCMOS 0.18 μ , 1-poly 6-metal, TowerJazz
- BCDMOS 0.18 μ , 1-poly 3-metal(MT), TowerJazz

- Coordinating chip fabrication services

- CMOS through CMP: 90-, 65-, 45-nanometre CMOS (STMicroelectronics)
- CMOS through Europractice : 90-nanometre CMOS(TSMC)
- CMOS through MOSIS: 90-, 65-, 45-nanometre 0.13-micron (IBM)

In 2011, IDEC started new chip fabrication services of Samsung 65nm and Dongbu 110nm CMOS process. IDEC is also going to provide a new fabrication process of Bongbu 0.18um BCDMOS in 2012.

Students who fabricate chips using IDEC MPW service are required to give posters/demo presentations in the IDEC Chip Design Contest. The contest is structured to promote excellence in the design of IPs and SoCs by guiding competition between students from universities and colleges. IDEC has also hosted the annual IP Design Contest supported by Dongbu HiTek since 2007, marking this year (2012) as the fifth year of the contest. These are good opportunities for students to introduce new IPs and design activities undertaken in their laboratories. IDEC supports registration for patents and IPs and intends to link industries and universities for IP based design technology development.

Along with these activities, about 4,000 copies of CAD Tools are supported to Working Groups every year by IDEC. Also CAD & Design Methodology Award was held to exchange new ideas, discuss problems and learn the usages of CAD Tools. IDEC has offered more than 3,062 lectures, seminars, and CAD tool training sessions. More than 79,888 people have registered overall in IDEC's educational programs. "2nd International Workshop on IT and Future Society" was held on November 16th at Jeju island in Korea by IDEC. There were the diagnostics of IT and suggestions on how to prepare for the future society as unfolded by 6 invited experts.

Moreover, IDEC published the first annual report including fabricated chips through IDEC and monthly newsletter, distributed to about 2,300 subscribers, to provide information about the IC design field.

As of 2012, participants of IDEC included 335 professors in 68 working groups (WGs) from 66 participating universities. Seven regional centers located in Chonbuk National University, Chonnam National University, Chungbuk National University, Hanyang University, Kwangwoon University, Kyungpook National University, and Pusan National University are cooperating with IDEC for realizing better performance.

Two IPCs (IDEC Platform Centers) were established at Kwangwoon University and Hanyang University last year (2011). They are to maximize the synergy effect with chip design, embedded software, and system design by building professional platforms on specified subjects. The third IPC is going to be established this year (2012).

Since 2009, we have annually been publishing and distributing "Technology Map of chip design platform" which shows WG professors' field of research. This map is contributing to research competitiveness by promoting joint researches between universities and communities.

Taiwan

National Chip Implementation Center (CIC) has been serving the academia in Taiwan since 1992. CIC has been providing chip design and implementation services as well as technology promotion to meet its mission of advancing IC/system design technology and developing high-caliber IC/system designers. For the past two decades, CIC has endeavored to provide academia in Taiwan services in the following three major areas: IC/system design environments; chip fabrication, heterogeneous packaging and measurement services; promotion of technology for IC/system design and international collaboration.

With the vision of being a world-class research and service center for IC/system design, CIC focuses on the following:

1. Train highcaliber IC/system design engineers
2. Develop advanced IC/system design technology

In 2011, the process technologies provided by CIC are listed below

- TSMC 90nm 1P9M RF Low Power CMOS
- TSMC 40nm 1P9M CMOS
- TSMC 90nm 1P9M MS General Purpose
- TSMC 0.18µm 1P6M CMOS
- TSMC 0.35µm 2P4M CMOS
- CMOS MEMS post-process based on TSMC 0.35 µm 2P4M CMOS process
- CMOS BioMEMS post-process with a new gold layer added based on TSMC 0.35 µm 2P4M CMOS process
- CMOS MEMS post-process based on TSMC 0.18 µm 1P6M CMOS process
- TSMC 0.18µm SiGe BiCMOS
- WIN 0.15µm PHEMT/MHEMT
- TSMC 0.25µm 60V High Voltage
- tMt GIPD

Currently, CIC offers process environment that includes design kits, design rules, and model files, etc. Furthermore, in order to confirm the feasibility of utilizing the technical data in EDA environment, CIC verifies the compatibility of EDA environment through real circuit. For easy application of using the environment, all the verified environment and data about processes can be downloaded from the website of CIC. In addition, CIC also provided relevant training courses to facilitate circuit design by designers using the aforementioned environments. In 2011, the advanced and educational chips taped out by the academia via CIC has reached a total amount of 1718.

To assist domestic academic circles in researching chip and system, CIC has introduced various popular design tools to teachers and students. Recently, together with demand for improvements in process technique and SoC design, individual EDA companies have continually updated their software and enhanced functions. CIC has also made arrangements with well-known EDA companies in integrating various design flows.

Besides, CIC offers measurement and verification services including general equipment, communication chip measurement, analog measurement and MEMS measurement services. Others like laser cutter, wire bonder, power supplier, LCR meters can all be linked by an automatic control system. As for MEMS chip measurement, besides keeping existing measurement service, new measurement instruments and technologies are developed as well. Furthermore, CIC has set up the Agilent 93000 SoC test system with 320 digital channels and 660 Mbit/s for each channel. Totally, CIC measurement and verification service has provided testing services to 1,339 projects in 2011.

Lastly, CIC also provides IC design related training courses and e-Learning courses. In 2011, CIC offered 175 training courses and most of courses were lectured by CIC staff members. 8,620 participants attended CIC's training courses in 2011.

USA

Introduction

MOSIS is a low-cost prototyping and small volume production service for VLSI circuit development with a worldwide customer base. Since 1981, the service has fabricated more than 50,000 integrated circuit designs for use by commercial firms, government agencies and universities and has served as the model for similar operations throughout the world. It is a not-for-profit organization started in 1980 by DARPA (Defense Advanced Research Projects Agency of the U.S. Department of Defense) at the University of Southern California's Information Sciences Institute to provide their research community with access to advanced IC fabrication lines in a cost effective manner. The cost reductions were the result of the use of the Multi-Project-Wafer (MPW) concept in a single fabrication run, where the fabrication cost is shared among all the users. In 1986, the service was further expanded to include U.S. commercial firms and in 1995 to include both commercial firms and educational institutions outside the U.S. Since 1994, MOSIS has been entirely self-supported, deriving all of its revenue from commercial operations.

Industrial Program

As described in the introduction, MOSIS derives all of its current revenues from commercial sources. A listing of the fabrication run schedules (regularly scheduled MPW runs; dedicated runs at customer's discretion), available technologies (CMOS 0.7 μ to 32nm, SiGe BiCMOS 0.5 to 0.13 μ ; CMOS HV), design kits and other requirements can be accessed through our web site. The MOSIS customer profile ranges from small companies with less than 50 employees (approximately 45% of industrial firms), to large industrial firms with more than 500 employees (approximately 40%) as well as various research laboratories worldwide.

Educational Program

In addition to the commercial work that supports the service, MOSIS operates an educational program open to universities worldwide. The program is divided into two major parts: (1) Projects designed by students enrolled in VLSI design classes at accredited universities and (2) Research projects from universities which are not funded by other sponsors. In the ten-year period from 2000 to 2009, MOSIS processed a total of nearly 7000 student IC designs from universities in the US at no cost to the participating universities. These designs came from VLSI classes totaling more than 38,000 students in beginning and advanced VLSI design classes. A MOSIS Advisory Panel for Education consisting of professors from U.S. universities and members of contributing industrial concerns provide guidance and direction to the educational program as well as identifying and securing sources of funding.

The fabrication of the educational projects is done at no cost to the participating universities. Funding for the Educational program is provided through contributions from the Semiconductor Research Corporation (SRC)

and industrial firms (IBM, ON Semi). The administrative expenses of the program as well as a portion of the operating expenses are provided by the MOSIS Service.

Available Technologies

Fast-turnaround prototype and low-volume fabrication of integrated circuits is available through a number of major commercial IC fabrication vendors such as GlobalFoundries (0.35 μ , 0.18 μ , 65nm CMOS), ON Semiconductor – was AMIS (0.35 μ , 0.5 μ , 0.7 μ CMOS), IBM (32nm, 45nm SOI; 65nm, 90nm, 0.13 μ , 0.18 μ and 0.25 μ CMOS; 0.13 μ , 0.18 μ , 0.25 μ , 0.35 μ and 0.5 μ SiGe BiCMOS) and TSMC (40nm, 65nm, 90nm, 0.13 μ , 0.18 μ , 0.25 μ , 0.35 μ CMOS). CMOS-compatible MEMS technologies are also available. Other technologies such as austriamicrosystems (0.35 μ CMOS, 0.35 μ HV CMOS, 0.35 μ SiGe BiCMOS) are available through a partnership with CMP in France.

The operation of the MOSIS Service is highly automated. Designs are received electronically, both from universities and from commercial sources. The designs are automatically placed in a queue for the requested technology by the system's front end, and the transaction records as well as the fabrication parameters are automatically validated (The system checks for valid account and other administrative details). The fabrication runs are conducted on a regular schedule, which is published and distributed for a minimum of a six-month period. Low volume production runs are processed whenever the customer is ready. The MOSIS service handles all the details of merging of the projects and generates all the necessary information to produce the required phototooling. For additional details please consult the MOSIS web site at <http://www.mosis.com/>

H – Cooperation with other services

Cooperative agreements

CMP has signed cooperative agreements with the following Institutions over the time:

- CIC, Taiwan
- FAPESP, Brazil
- Royal Institute of Technology, Sweden
- ICC, China
- IDEC, Korea

CMP Distributors

- Meds - Singapore
- Sevia Multimedia Technologies Pvt. Ltd.– India
- Waken – Japan
- SiliConsortium Ltd. - Japan

Collaboration CMC – CMP – MOSIS

From 2001 the three main ICs manufacturing services from USA (MOSIS), Canada (CMC) and France (CMP) started a partnership in order to exchange some of their services and to enlarge the portfolio of technologies proposed by each partner. In this way technologies from austriamicrosystems and OMMIC were offered to MOSIS customers and technologies from Peregrine, IBM and Vitesse were offered to CMP customers. This program was still developed in 2007 (see Appendix 14), in particular for MEMS: many circuits were fabricated through CMP for CMC (Canada) Institutions. Such program is necessary to support escalating costs of very deep sub-micron processes or the low demand of very specialized processes.