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Chapitre
Français

Design-Kits, Libraries & IPs



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- Supported CAD tools
- Design-kits overview
- Digital, Analog, and RF Libraries
- IPs



STMicroelectronics

- Design-kits overview by process
- Standard cell Libraries
- IPs



Design-kits & IPs support at CMP



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- **0.35 μ m CMOS**
- **0.35 μ m SiGe**
- **0.35 μ m HV-CMOS**
- **0.8 μ m BICMOS**



austriamicrosystems Supported CAD Tools



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	Schematic & Design Entry	Electrical Simulation	Digital Simulation	Logic Synthesis	Layout & Verification	P&R
Cadence	Composer (CDS)	Spectre (CDS) Hspice Ultrasim	NC-Sim, AMS-Designer Verilog	BuildGates	Virtuoso-XL Diva Assura	SOC Encounter ICC Silicon Ensemble
Mentor	DA (MGC)	Eldo (MGC)	ModelSim	Leonardo	IC / Calibre	IC-Route
Synopsys	Design Compiler	Hspice	VSS / VCS	Design Compiler	StarRCXT	Astro
Tanner	S-Edit	TSpice	TSpice	---	L-Edit DRC	SPR
		Pspice (CDS)				
		Saber (Synopsys)				
		ADS (Agilent)				
		Smash (Dolphin)				
		SmartSpice (Silvaco)				



● Current distributions :

	Cadence (SUN / HP / Linux)	Mentor (SUN / Linux)	Tanner (MS-Windows)
0.8 μ m BiCMOS	3.70		
0.35 μ m CMOS	3.70 4.0	3.70	5.0
0.35 μ m SiGe	3.70 4.0	3.70	
0.35 μ m HV-CMOS	3.72 4.0	3.71	



For Cadence 6.1.2



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Digital standard cells and IO Libraries :

- CORELIB : General purpose digital library
- CORELIB_3B : Same as CORELIB with 3 busses (VDD, VSS, GND)
- CORELIB_HV : CORELIB for high voltage.
- IOLIB : IO pads (input, output, bidir). 3.3V and 5V available
- IOLIBC_3B : Core limited digital IO Libraries
- IOLIB_HV : High Voltage digital IO pads library

Analog standard cells Libraries :

- IOLIB_ANA : Analog IO pads library
- IOLIBC_ANA_3B : Core limited Analog IO pads library
- IOLIB_ANA_HV : High Voltage Analog IO pads library
- A_CELLS : Analog Library (available with license fees)

RF standard IO cells Libraries :

- SPIRAL : Library with characterized Inductors
- RF_PADS : RF IO pads library



IP blocks available from CMP free of charge to Univ. & Research (0.35µ CMOS)

Single & Dual Port RAMS configurations:

Words \ Bits	8	9	12	16	32
128	SP	SP	SP		SP
256	SP / DP			SP / DP	
512				SP	SP
600				SP	
1024	SP / DP			SP / DP	
2048	SP			SP / DP	SP
4096	DP				

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Generate a Memory Simulation Model

For more information about memory blocks and possible configurations please take a look at [Digital Macros & Blocks](#)

Please contact your local sales representative to order the generation of the final memory layout data.

Before you start, please check your [Profile](#)

Please specify your memory



Process: C35
 Metalization: Triple Metal
 Voltage: 3.3V
 Model: Single Port RAM
 Data Bus: Separated Inputs and Outputs
 Number of Words:
 Number of Bits/Word:

Estimate Reset

Single Port RAM
 Dual Port RAM
 Diffusion ROM



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- HCMOS9 (*130nm CMOS*)
-  • HCMOS9-SOI (*130nm CMOS-SOI*)
- CMOS090 (*90nm CMOS*)
- CMOS065 (*65nm CMOS*)
-  • CMOS065-SOI (*65nm CMOS-SOI*)
- CMOS045 (*45nm CMOS*)
- BiCMOS7RF (*0.25 μm SiGe*)



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HCMOS9 Design-kit



● Complete Design-kit For Cadence 5.1.41:

Full-custom :

Cadence/Composer schematic Editor

Spectre, Eldo, Hspice

Cadence/Virtuoso-XL Layout, & ICC.

Calibre & Diva Verifications (Calibre is the Sign-off)

StarRCXT

Diva Parasitics Extraction (available from CMP)

Standard cells :

- Several CORE libraries (HS/LL and LL/ULL). (About 700 cells per library).
- IO pad libraries with digital and analog pads (2.5V and 3.3V).
- P&R available for Synopsys Backend tools.
- P&R for SoC Encounter. **(available from CMP)**
- Memories SPRAM / DPRAM / MPRAM / ROM available on request, *free of charge* (1-2 weeks delay)

● RF option available.



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HCMOS9-SOI Design-kit



● Design-kit For Cadence 5.1.41:

Full-custom :

Cadence/Composer schematic Editor
Spectre, Eldo, Hspice
Cadence/Virtuoso-XL Layout, & ICC.
Calibre Verifications
StarRCXT



CMOS090 Design-kit



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● Complete Design-kit For Cadence 5.1.41:

Full-custom :

Cadence/Composer schematic Editor
Spectre, Eldo, Hspice
Cadence/Virtuoso-XL Layout, & ICC.
Calibre Verifications
StarRCXT

Standard cells :

- 3 sets of CORE libraries (HVT, SVT, LVT). (About 1000 cells per library).
- IO pad libraries with digital and analog pads (2.5V and 3.3V).
- P&R available for Synopsys Backend tools.
- P&R for SoC Encounter.
- Memories SPRAM / DPRAM / ROM available on request, *free of charge* (1-2 weeks delay)

● RF option available.



CMOS065 Design-kit



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● Complete Design-kit For Cadence 5.1.41:

Full-custom :

Cadence/Composer schematic Editor
Spectre, Eldo, Hspice
Cadence/Virtuoso-XL Layout, & ICC.
Calibre Verifications
StarRCXT

Standard cells :

- 3 sets of CORE libraries (HVT, SVT, LVT). (About 1000 cells per library).
- IO pad libraries with digital and analog pads (1.8V and 2.5V).
- P&R available for Synopsys Backend tools.
- P&R for SoC Encounter.
- Memories SPRAM / DPRAM / ROM available on request, *free of charge* (1-2 weeks delay)

● RF option available.



● Complete Design-kit For Cadence 5.1.41:

Full-custom :

Cadence/Composer schematic Editor
Spectre, Eldo, Hspice
Cadence/Virtuoso-XL Layout, & ICC.
Calibre Verifications
StarRCXT

Standard cells :

- 2 sets of CORE libraries (HVT, LVT).
- IO pad libraries with digital and analog pads (2.5V).
- P&R available for Synopsys Backend tools.



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CMOS045 Design-kit



● Complete Design-kit For Cadence 5.1.41: Full-custom :

Cadence/Composer schematic Editor
Spectre, Eldo, Hspice
Cadence/Virtuoso-XL Layout, & ICC.
Calibre Verifications
StarRCXT

Standard cells :

- Several CORE libraries.
- IO pad libraries with digital and analog pads (1.8V).
- P&R available for Synopsys Backend tools.
- P&R for SoC Encounter.
- Memories SPRAM / DPRAM / ROM available on request, *free of charge*
(1-2 weeks delay)



● CAD tools - Digital:

- **Design Compiler** (*Synthesis*)
- **NCSim & Modelsim** (*Digital Simulation*)
- **Formality** (*Functional Verification*)
- **Primitime** (*Static Timing Analysis*)
- **Apollo/Astro** (*Floorplanning, Physical Synthesis, Clock Synthesis & Route*)
- **StarRCXT** (*Parasitics Extraction*)
- **Dsqpf2dspf** (*Si/Xtalk*) - ST tool

● CAD tools – Analog/Mixed:

- **Opus** (*Analog Frameworks*)
- **Composer** (*Schematic capture*)
- **Analog Artist** (*Analog Simulation Env.*)
- **Eldo, Spectre** (*Analog Simulation*)
- **ADMS** (*Mixed Simulation*)
- **NCSim & Modelsim** (*Digital Simulation*)
- **Epic & ADVance-MS** (*Top Level Simulation*)
- **Cadence/Virtuoso-XL Layout & ICC** (*Layout Editing*)
- **Calibre** (*DRC/LVS*)
- **StarRCXT** (*Parasitics Extraction Analog*)



● CORE cells Libraries :

- CORE : General purpose core libraries
- CORX : Complementary core libraries (complex gates)
- CLOCK : Buffer cells and the same for clock tree synthesis
- PR : Place and route filler cells and the same.
- ~~DP : Datapath leaf cells libraries~~
- ~~HD : High density core libraries~~ } on request

● IO cells Libraries :

1.8V, 2.5V, 3.3V IO pads:

- 80 μ , 65 μ , 60 μ , 50 μ 40 μ and 30 μ IO pads : Digital and Analog
- Staggered IO pads
- Flip-Chip pads
- LVDS Pads

On request:

- Level Shifters, and compensation cells
- OUTDIFF : Differential output pads
- DLL, PLL
- ...



IP Blocks Available from STMicroelectronics



- **ARM 946EJ-S :**

 - HCMOS9 0.12u CMOS IP core

 - Simulation models

 - Abstract view for P&R

 - Timing Files for STA and backannotated simulation

 - Available under NDA

- **ARM 926EJ-S :**

 - CMOS065 65nm CMOS IP core

 - Simulation models

 - Abstract view for P&R

 - Timing Files for STA and backannotated simulation

 - Available under NDA

+ Access to all available ARM cores in 65nm.



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Design-Kit Support at CMP



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- Management and support of the DK distribution and updates.
- Development, support and maintenance of design-kits.
- Two engineers work partly at ST to solve all kind of support with ST design-kits and memory blocks generation.
- Management and support of the ARM IP core access.