



0.18 μm High-Voltage CMOS Process (H18)

Full Service Foundry
January 2011

HV processes at austriamicrosystems

Definition:

At austriamicrosystems, High-Voltage means ALL voltage domains higher than 5V !

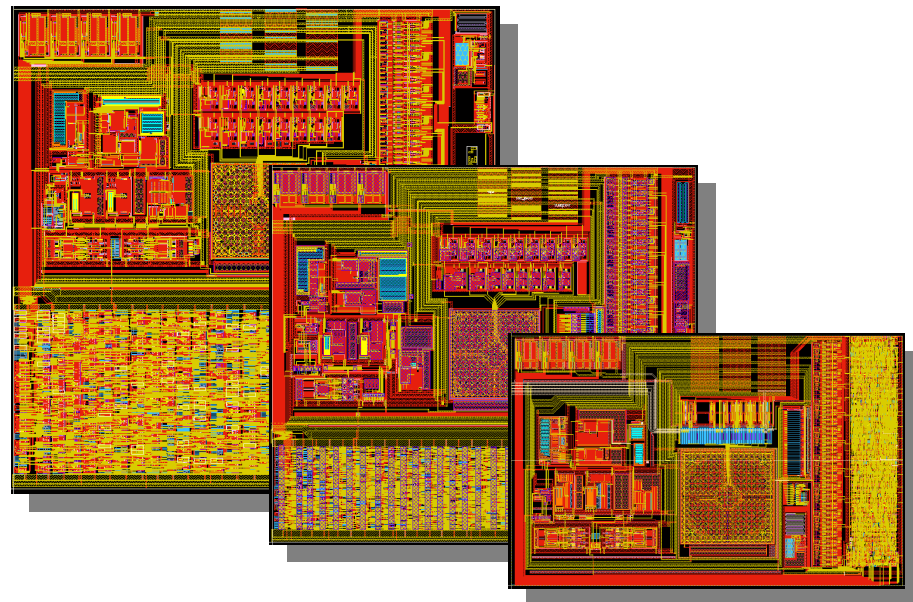
Available High-Voltage processes:

2.0 μ m – **CBZ**: 50V

0.8 μ m – **CXZ**: 50V

0.35 μ m – **H35**: 20V, 50V, 120V

0.18 μ m – **H18**: 20V, 50V



H18 - Key technology features

- CMOS technology with ≤ 3 mask level adders for HV
- Three gate oxides available: 1.8, 5V and 20V
- 4 to 7 metal levels (last metal: 4 μm Al power metal)
- Full set of 20 V and 50 V LDMOS devices
- Low R_{dson}
 - $< 14 \text{ m}\Omega \cdot \text{mm}^2 @ 30 \text{ V BVDSS}$
 - $< 130 \text{ m}\Omega \cdot \text{mm}^2 @ 70 \text{ V BVDSS}$
- 1.8 V and 5 V floating logic (N/PFET)
- High-voltage vertical NPN & PNP bipolar transistors
- Isolated JFET
- High-voltage VN capacitors (20-50V)
- High voltage well based resistors
- 1 kV, 2 kV and 4 kV HBM ESD protection structures
- OTP (Efuse)
- Tool for safe operating area check (SOAC)



H18 device list

Existing 7RF Devices

Thin oxide NFET/PFET 1.8V
 Medium oxide NFET/PFET 5V
 High Vt NFET/PFET 1.8V
 N+ diffusion resistor
 P+ diffusion resistor
 N+ poly resistor
 P+ poly resistor
 K1 BEOL resistor
 High resistivity poly resistor
 precision poly resistor
 Single Nitride MIM
 Dual Nitride MIM
 HighK MIM
 PCDCAP thin ox
 Vertical parallel plate capacitor (VNcap)
 Schottky Barrier Diode
 Efuse
 Bondpad



Modifications to existing devices for HV process:

Thin oxide NFETi/PFETi 1.8V in HV wells
 Medium oxide NFETi/PFETi 5V in HV wells
 High Vt NFETi/PFETi 1.8V in HV wells
 N+ diffusion resistor in HV well
 P+ diffusion resistor in HV well

New Devices:

Thin oxide NFETi/PFET 20V
 Thick oxide NFETi/PFET 20V
 Thick oxide NFETi/PFET symmetric 20V
 Medium oxide NFETi 20V
 Medium oxide NFETi/PFET 25V
 Thin oxide NFETi/PFET 50V
 Medium oxide NFETi/PFET 50V
 Thick NFETi/PFET 50V
 Thick NFETi/PFET symmetric 50V
 3 terminal JFET
 Parasitic VPNP (high V)
 Parasitic VNPN (isolated)
 NWell resistor in HV well
 PWell resistor in HV well
 High Voltage VNcap

Suite of FETs with three gate oxide thicknesses

- Low Voltage (LV) fets for standard 1.8 and 5V CMOS
- LV fets in HV well for high voltage isolation to substrate
- HV asymmetric fets for High Voltage applications
- -3 gate oxide thicknesses, 2 maximum drain bias choices
- HV symmetric fets for specialty applications (transmission gate)

	LV fets		LV fets in HV well		HV asymmetric fets in HV wells		HV symmetric fets (nfet in Substrate)	
Vds \ Vgs	1.8V	5.0V	1.8V	5.0V	20V**	50V	20V	50V
1.8V (3.5nm)	nfet* pfet* nfethvt pfethvt		nfeti* pfeti* nfetihvt pfetihvt		nfeti20t pfet20t	nfeti50t pfet50t		
5.0V (12nm)		nfetm pfetm		nfetim pfetim	nfet20mh nfeti25m pfet25m	nfeti50m pfet50m		
20V (52nm)					nfeti20h pfet20h	nfeti50h pfet50h	nfet20hs pfet20hs	nfet50hs pfet50hs

* RF layout available ** 25V Vds for nfeti25m,pfeti25m

H18 Low Voltage Key Facts

Technology: Logic & HV		
Core Voltage	1.8	V
IO Voltage	5	V
HV Gate Voltage	20	V
RO Speed	28	ps/gate

Geometry 180nm		
Gate Dielectric tox (core)	3.5	nm
Gate Dielectric tox (IO)	12	nm
Gate Dielectric tox (HV)	52	nm
Emb-6T SRAM cell	3.6	μm²

Device Characteristics (Core)		
VDD	1.8	V
n/pFET - I _{dsat}	600 / -260	μA/μm
n/pFET - V _t	0.35 / -0.42	V
n/pFET - I _{leak}	<300 / <-300	pA/μm
n/pFET HVT - I _{dsat}	500 / -210	μA/μm
n/pFET HVT - V _t	0.52 / -0.52	V
n/pFET HVT - I _{leak}	<30 / <-30	pA/μm

Device Characteristics (IO)		
VDD	5.0	V
n/pFET - I _{dsat}	630 / -350	μA / μm
n/pFET - V _t	0.63 / -0.65	V
n/pFET - I _{leak}	<15 / <-22	pA / μm

H18 Passives Key Facts

Resistors		
N+ diffusion resistor	72	$\Omega / \#$
P+ diffusion resistor	105	$\Omega / \#$
TaN resistor	61	$\Omega / \#$
N+ poly resistor	370	$\Omega / \#$
P+ poly resistor	260	$\Omega / \#$
hires poly resistor	1600	$\Omega / \#$
Precision poly resistor	165	$\Omega / \#$
TaN resistor	61	$\Omega / \#$
HV Nwell resistor	3074	$\Omega / \#$
HV Pwell resistor	725	$\Omega / \#$

Capacitors		
Single MIM capacitor	2.05	fF / μm^2
Single MIM HD capacitor	2.7	fF / μm^2
Dual MIM capacitor	4.1	fF / μm^2
Dual MIM HD capacitor	5.4	fF / μm^2
HiK MIM capacitor	4.1	fF / μm^2
VN capacitor	0.1-0.7	fF / μm^2
HV VN capacitor	0.1-0.5	fF / μm^2

H18 High Voltage FET Devices

Parameter	Asymmetric, thinnest oxide, isolated well		Asymm., med. oxide in substrate	Asymmetric, medium oxide, isolated well		Asymmetric, thickest oxide, isolated well		Symmetric, thickest oxide, in substrate	
	nfeti20t	nfeti50t	nfet20mh	nfeti25m	nfeti50m	nfeti20h	nfeti50h	nfet20hs	nfet50hs
Min Drain-source breakdown (V)	29	83	27	33	73	28	79	32	85
Tox (physical, nm) / Max VGS (V)	3.5 / 1.98	3.5 / 1.98	12 / 5.5	12 / 5.5	12 / 5.5	52 / 20	52 / 20	52 / 20	52 / 20
Ldrawn (μm)	0.2	0.2	0.4	0.4	0.4	0.5	0.5	0.7	1.3
V _T (short wide V)	0.43	0.40	0.80	0.71	0.72	2.0	2.14	2.15	2.15
IDSat (μA/ μm)	200	172	400	343	266	580	353	340	230
On Resistance mΩ-mm ²	35.1	168	17.1	45.2	143	29.5	138	47.1	316
On Resistance mΩ-mm ² (butted)*	29.8	155	14.4	39.2	132	25.5	128		

Parameter	Asymmetric, thinnest oxide		Asymmetric, medium oxide		Asymmetric, thickest oxide		Symmetric, thickest oxide	
	pfet20t	pfet50t	pfet25m	pfet50m	pfet20h	pfet50h	pfet20hs	Pfet50hs
Min Drain-source breakdown (V)	-30	-70	-32	-70	-35	-70	-28	-70
Tox (physical, nm) / Max VGS (V)	3.5 / 1.98	3.5 / 1.98	12 / 5.5	12 / 5.5	52 / 20	52 / 20	52 / 20	52 / 20
Ldrawn (μm)	0.2	0.2	0.6	0.6	0.6	0.6	2.0	3.0
V _T (short wide V)	-0.35	-0.35	-0.51	-0.52	-2.48	-2.52	-1.80	-1.80
IDSat (μA/ μm)	140	123	220	204	345	309	250	160
On Resistance mΩ-mm ²	53.0	187	66.0	194	63.0	183	129	630
On Resistance mΩ-mm ² (butted)*	41.8	166	53.8	174	51.7	166		

H18 – 0.18 μ m High Voltage CMOS

Technology Availability Status

- Process in qualification (jointly with IBM)
- First silicon based HIT-Kit in June 2008, final HIT-Kit in Q4/2010
- Full production release in Q1/2011
- **Customers welcome NOW !**

Top Benefits

- High performance HV CMOS matching BCD performance
- Several voltage regimes on one chip enables optimized area

Target Applications

- Power management applications
- MEMS and Sensor interfaces
- Other SOC applications in Medical, Automotive and Industrial

Process Details

- **1,8V / 5,0V / 20V / 50 V**
- **Gate Density: 118 kGates per mm²**
- **Low power & low leakage digital libraries**

Best in class!

Process Design Kit (HIT-Kit)

HIT-Kits are Cadence PCell based

- Included for every device: symbolic symbol, layout parameterized cell, and verified device models
- Limits device usage to well understood parameter-space

Simulation options include:

- Cadence Analog Design Environment – Spectre and HSPICE

Physical verification tools include Assura & Calibre

Parasitic extraction options

- QRC RCX (R, L & C)
- Calibre xRC (R, L & C)
- Star RCXT (per customer request)

HIT-Kit also include SKILL automation code

- Design migration code (version-to-version)
- Launch verification runs

Supported Tools

Tool/Technology	IBM 7RF	H18
Cadence Device Library	Y	Y
Cadence Assura DRC	Y	Y
Cadence Assura LVS	Y	Y
Cadence QRC RCX	Y	Y
Mentor Calibre DRC	Y	Y
Mentor Calibre LVS	Y	Y
Mentor Calibre xRC	Y	Y
Synopsys Hercules DRC	Y	N
Synopsys Hercules LVS	Y	N
Synopsys Star RCXT	Y	Y
Columbus AMS	Y	N
Spectre Models	Y	Y
HSPICE Models	Y	Y
Agilent ADS	Y	N
Mentor Eldo	Y	N

austriamicrosystems MPW Service

MPW Schedule 2011

⇒ <http://asic.austriamicrosystems.com/MPW>

Process	Data and Order to	Tape In	Samples Out ⁶⁾
0.18 μm HV-CMOS 20V / 50V ⁸⁾			
H18	<i>austria micro systems</i>	14-Feb-11	22-Apr-11
H18	<i>austria micro systems</i>	02-May-11	22-Jul-11
H18	<i>austria micro systems</i>	01-Aug-11	07-Oct-11
H18	<i>austria micro systems</i>	28-Nov-11	03-Feb-12
0.18 μm CMOS 1.8V / 2.5V / 3.3V (5V ⁷⁾)			
C18	<i>austria micro systems</i>	14-Feb-11	22-Apr-11
C18	<i>austria micro systems</i>	18-Apr-11	24-Jun-11
C18	<i>austria micro systems</i>	06-Jun-11	12-Aug-11
C18	<i>austria micro systems</i>	15-Aug-11	21-Oct-11
C18	<i>austria micro systems</i>	10-Oct-11	16-Dec-11
C18	<i>austria micro systems</i>	05-Dec-11	10-Feb-12
0.35 μm HV-CMOS 20V / 50V / 120V (embedded Flash ⁵⁾)			
H35B4D3	<i>austria micro systems</i>	21-Feb-11	22-Apr-11
H35B4D3	<i>austria micro systems</i>	02-May-11	01-Jul-11
H35B4D3	<i>austria micro systems</i>	16-Aug-11	14-Oct-11
H35B4D3	<i>austria micro systems</i>	14-Nov-11	14-Jan-12
0.35 μm CMOS 3.3V / 5V (embedded Flash ⁵⁾) and 0.35 μm Opto-CMOS ²⁾			
C35 ¹⁾	<i>austria micro systems</i>	14-Feb-11	01-Apr-11
C35 ^{1) 2)}	Fraunhofer IIS	11-Apr-11	01-Jun-11
C35 ¹⁾	<i>austria micro systems</i>	30-May-11	15-Jul-11
C35 ¹⁾	Fraunhofer IIS	18-Jul-11	09-Sep-11
C35 ¹⁾	<i>austria micro systems</i>	05-Sep-11	21-Oct-11
C35 ^{1) 2)}	Fraunhofer IIS	02-Nov-11	14-Dec-11
C35 ¹⁾	<i>austria micro systems</i>	12-Dec-11	27-Jan-12
0.35 μm SiGe-BiCMOS 3.3V / 5V 2P/4M			
S35	<i>austria micro systems</i>	07-Mar-11	06-May-11
S35	<i>austria micro systems</i>	14-Jun-11	12-Aug-11
S35	<i>austria micro systems</i>	12-Sep-11	11-Nov-11
S35	<i>austria micro systems</i>	28-Nov-11	27-Jan-12

Summary


austriamicrosystems new 0.18 μ m High-Voltage CMOS technology H18 is optimized for integrated power applications:

- Offers cost and time-to-market advantages
- Provides excellent analog performance
- Allows flexible use of high-voltage transistors

austriamicrosystems is ready to help you succeed!

- 25+ years experience in analog mixed signal technology
- More than 15 years experience in High-Voltage design
- Industry-leading analog design environment (HIT-Kit)
- Experienced technical support
- High-quality manufacturing





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