

STMicroelectronics

Deep Sub-Micron Processes
130nm, 65 nm, 40nm CMOS

SOI Processes
130nm, 65 nm

SiGe
130nm



CMP Process Portfolio from ST



Moore's Law

130nm CMOS : HCMOS9GP

65nm CMOS : CMOS065

40nm CMOS : CMOS040LP

32nm CMOS : CMOS032LP

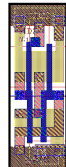
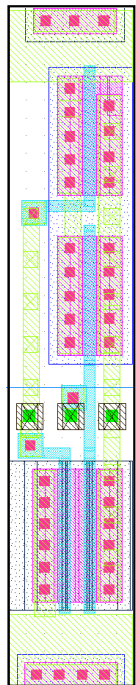
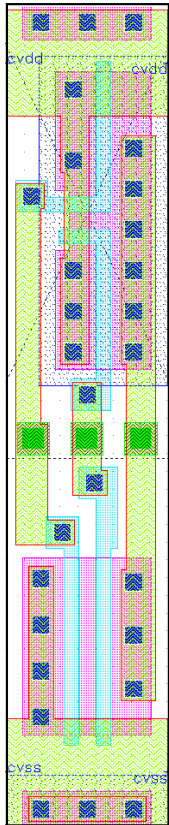
More than Moore

130nm SiGe : BICMOS9MW

65nm SOI : CMOS065-SOI

130nm SOI : HCMOS9-SOI

- 1300 x density integration
- 1/1000 x gate delay (from ns to ps)
- 1/1000 x power consumption (from $\mu\text{W}/\text{MHz}$ to nW/MHz)



AMS 0.8 μ	AMS 0.6 μ	AMS 0.35 μ	ST 0.25 μ	ST 0.18 μ	ST 0.13 μ	ST 90nm	ST 65nm	ST 40nm
1.2k gates/mm ²	3k gates/mm ²	18k gates/mm ²	35k gates/mm ²	80k gates/mm ²	180k gates/mm ²	400k gates/mm ²	800k gates/mm ²	1600k gates/mm ²

1994 at CMP



2010 at CMP



Process Roadmap



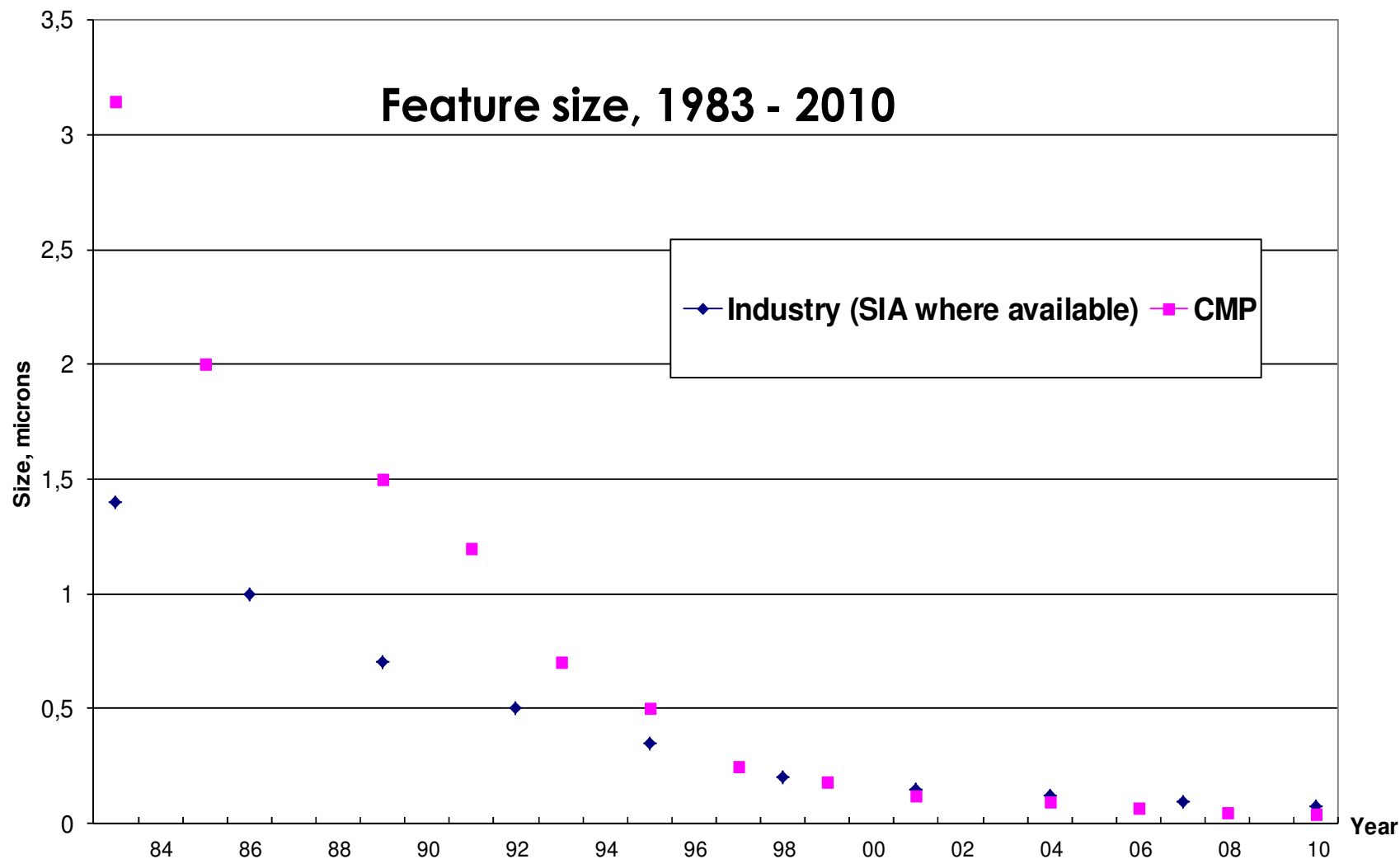
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CNRS - INPG - UJF

- Since 1997 CMP was continuously offering advanced processes
- 2010 and beyond is a new era with nanometer scale processes



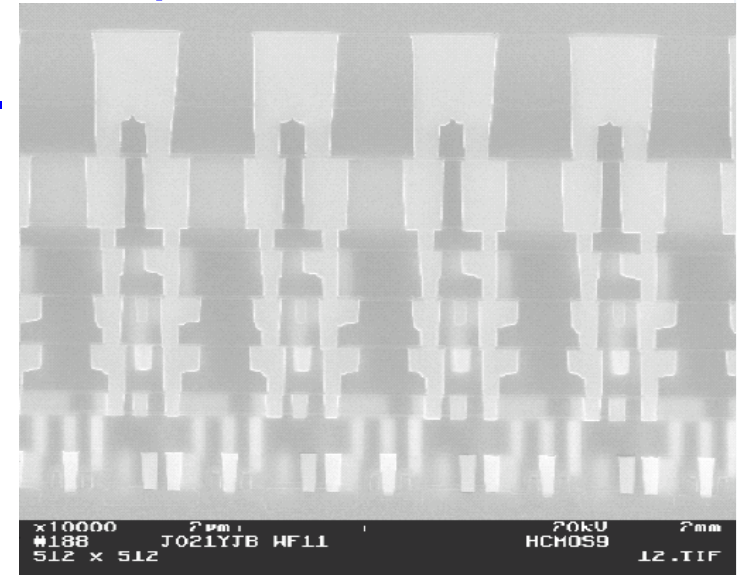


H9 C65 C40 C65 SOI H9 SOI B9 MW

STMicroelectronics ***CMOS 130nm***

HCMOS9

- 130nm mixed A/D/RF CMOS SLP/6LM (triple Well)
- Gate length (0.13 μm drawn, 0.11 μm effective).
- 6 Cu metal layers.
- Low k inter-level dielectric
- Power supply: 1.2 V
- Multiple Vt transistor offering
- (Ultra low leakage, low leakage, High speed)
- Threshold voltages (for 3 families above) :
- VTN = 570/500/380 mV, VTP = 590/480/390 mV
- Isat (for 3 families above) :
- TN @ 1.2 V : 410/535/680 $\mu\text{A}/\mu\text{m}$; TP @ 1.2 V : 170/240/320 $\mu\text{A}/\mu\text{m}$



6 levels Cu Metal (Cross Section View)
Courtesy STMicroelectronics



Designs Fabricated in 2010

**H9**

C65

C40

C65 SOI

H9 SOI

B9 MW

- **46** designs have been fabricated in 130nm CMOS in **2010**.
- From **22** customers :

North America (2)

- University of Virginia
- Columbia University

Asia (1)

- ETRI, Korea

Europe (19)

- Aalto University (Finlande)
- Chalmers University of Technology
- CIM-PACA
- CMP (consortium ANR/SPIN)
- ENSSAT Université de Rennes 1
- ETH Zentrum IIS
- IM2NP/L2MP Polytech Marseille
- IMS Bordeaux
- Instituto Microelectronica Sevilla (IMSE)
- LETI/CEA Grenoble
- Linköping University – ISY
- LIRMM Montpellier
- SUPELEC, Gif/Yvette
- Università degli studi di Pavia
- UCL Louvain
- Université de Bourgogne
- Univ. P&M Curie (Paris 6)
- University of Modena and Reggio Emilia
- University of Sevilla - Escuela Superior de Ingeniero



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

STMicroelectronics ***65nm CMOS***

CMOS065



CMOS065 CMOS 65nm Process Features



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

- 65nm poly length
- Dual or triple Vt MOS transistors
- Dual or triple gate oxide
- Dedicated process flavors for high performance or low power
- Dual-damascene copper for interconnect
- Low-k (k = 2.9) dielectric
- 6 or 7 metal layers for interconnect
- 0.20 micron metallization pitch
- Analog/RF capabilities
- Fully compatible with e-DRAM
- 800 kgates/mm²
- Various power supplies supported: 2.5V, 1.8V, 1.2V, 1V
- Available at CMP from Q4 2006



Designs Fabricated in 2007



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

- **23** designs have been fabricated in 65nm CMOS in **2007**.
- From **9** customers :

North America (4) **7 designs**

- CMC* (4)
- BWRC (1)
- Georgia Institute of Technology (1)
- University of California, Davis (1)

(*) 13 Canadian Universities

Europe (5) **16 designs**

- IMS-Bordeaux (7)
- ISEN Lille(1)
- ENST (1)
- LAAS (1)
- LETI / CEA Grenoble (6)



Designs Fabricated in 2008



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

➤ **32** designs have been fabricated in 65nm CMOS in **2008**.

➤ From **16** customers :

North America (5)

- CMC*
- BWRC
- University of Michigan
- University of Minnesota
- University of Virginia

(*) 15 Canadian Universities

Asia (1)

Nanyang Tech. Univ. (Singapore)

Europe (9)

- IMS-Bordeaux
- ISEN Lille
- ENST
- KU-Leuven
- LAAS
- LETI / CEA Grenoble
- Politecnico di Milano
- UPC Catalunya
- University of Stuttgart

Africa (1)

Univ. Of Pretoria (South Africa)



Designs Fabricated in 2009



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

➤ 60 designs have been fabricated in 65nm CMOS in 2009.

➤ From 24 customers :

North America (9)

- CMC* Canada
- Univ. of Calgary Canada
- BWRC Berkeley
- University of Michigan
- University of Minnesota
- Columbia University New York
- Arizona State University
- California University of Technology
- University of Virginia

(*) 18 Canadian Universities

Asia (2)

- Univ. of Tokyo
- Univ. of Macau

Europe (13)

- IMS-Bordeaux
- ISEN Lille
- ENST Telecom Paris
- UCL Louvain Belgium
- LAAS
- LETI / CEA Grenoble
- CMP Georges Charpak
- CIM- PACA
- UPC Catalunya
- Chalmers Univ. Of Tech.
- Lund Univ.
- Linköping University – ISY
- VTT Information Tech.



Designs Fabricated in 2010



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

- 57 designs have been fabricated in 65nm CMOS in 2010.
- From 27 customers :

North America (8)

- BWRC Berkeley
- MIT
- Columbia University New York
- University of Michigan
- UCLA
- University of Minnesota
- California University of Technology
- Carnegie Mellon University

Asia (1)

- Univ. of Macau

Europe (18)

- ECL, Lyon
- ENSSAT-UNIVERSITE DE RENNES 1
- IMS-Bordeaux
- LAAS Toulouse
- UCL Louvain Belgium
- LAAS Toulouse
- LETI / CEA Grenoble
- INVIA
- MENTA
- University di Padova
- University of Paderborn
- Linköping University – ISY
- VTT Information Tech.
- University of Wuppertal
- Tyndall National Institute
- UPC Catalunya
- Universidad Carlos II de Madrid
- Lund University



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

STMicroelectronics ***40nm CMOS***

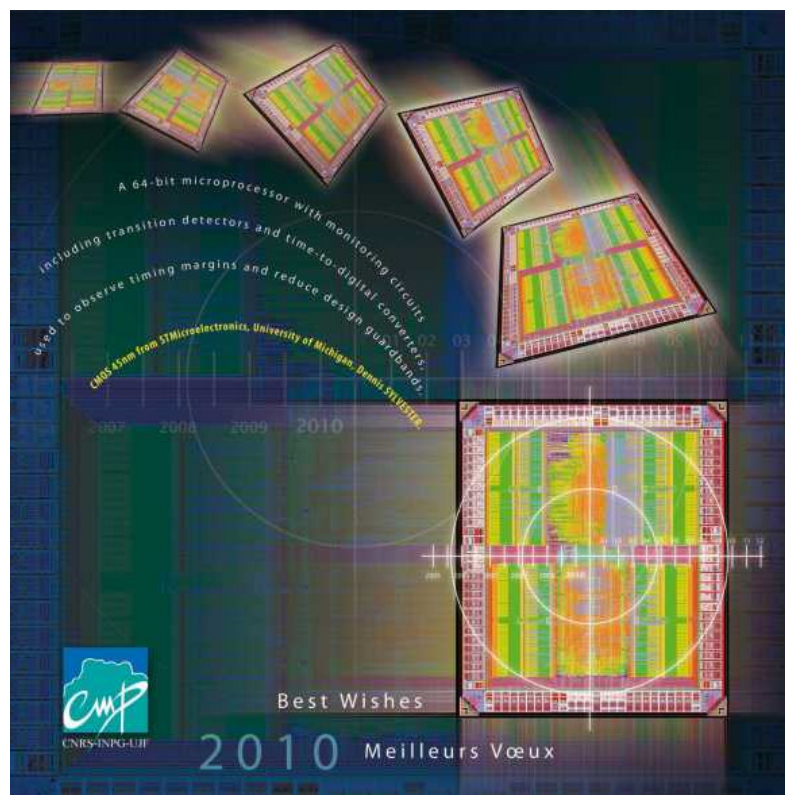
CMOS040LP



CMOS040LP Process Features :

- Multiple library elements can be selected at the design level and used in the same design block, providing users of the platform with greater flexibility in optimizing performance and power consumption.
- Densities of up to 1600 Kgates / mm², supporting a core supply of 1.1V, with metal pitches of 0.14-micron, and 7 metal layers.
- Power reduction techniques include adaptive *vdd*, low *vdd* operation, power shutdown, low standby current, etc ...
- Full range of 1.8V I/O cells.
- Extremely dense embedded memories: SRAM cells, with area sizes down to 0.25 square micron, at a supply voltage of 1.1V down to 0.9V

- 4 designs have been fabricated in 45nm CMOS in 2008.
- From 2 customers :
 - BWRC, Berkeley, USA
 - University of Michigan, USA





H9

C65

C40

C65 SOI

H9 SOI

B9 MW

BiCMOS9MW Process

130nm SiGe:C BiCMOS process

For millimeter wave, wireless, optical communications



BICMOS9MW Process Features



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

- BICMOS9MW technology is using 0.13 μ m HCMOS9 as base process.
- Address millimeterwave applications (frequencies up to 77GHz for automotive radar), wireless communication (frequencies around 60GHz for WLAN) and optical communications systems driving data rates up 80Gbit/s.
- SiGe-C bipolar transistor (fT around 230GHz)

Process Features :

- CMOS devices for 1.2V applications.
- 2.5V Capable I/O's.
- A high performance NPN bipolar transistor.
- A medium voltage NPN bipolar transistor.
- Shallow trench isolation (STI), triple well (NISO), twin-tub, single poly, for CMOS core process.
- Deep trench isolation (DTI) combined with STI and SiGe-C epi base for NPN transistors
- Optional Dual Vt
- Back-end with 6 metal layers.
- Damascene Copper for metal 1 to last metal.
- Thin metal layers : metal 1 to 3
- Thick metal layers : Metal4, Metal5 and Metal6.
- MIM capacitors



BICMOS9MW MPW runs



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

- 29 circuits manufactured in 2010
- MPW price is 3500 Euro/mm². (4500 Euro/mm² for industrial users)
- 4 MPW runs scheduled in 2011.



BICMOS9MW MPW runs in 2010



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

- **29** designs have been fabricated in 130nm SiGe in **2010**.
- From **12** customers :

North America (5)

- Peraso Tech. Inc, Toronto (Canada)
- BWRC Berkeley, USA
- Univ. of Calgary (Canada)
- Univ. of Toronto (Canada)
- California Institute of Technology
(Canada)

Europe (7)

- IMS-Bordeaux (FR)
- LAAS Toulouse (FR)
- Delft Univ. of Technology (NL)
- Acreo AB, (SE)
- Catena Holding B.V., Delft (NL)
- Thales S. A. Elancourt (FR)
- Philips Research, Eindhoven (NL)



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

SOI processes



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

CMOS065LP-SOI Process Features:

- Partially Depleted SOI on High Resistivity Substrate
- Triple-VT 1.2V transistors, with both floating body and Body-contacted versions
- 1 thick oxide for either 1.8V or 2.5V IOs
- 6 levels of metal (last metal is thick)
- RF-MOS, RF-PADS, varactors, inductors...
- MPW runs common to every CMOS065 bulk (3 MPW runs in 2011)



Designs Fabricated in 2009



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

- **27** designs have been fabricated in 65nm SOI in **2009**.
- From **9** customers :

North America (1)

- University of Massachusetts (USA)

Europe (8)

- IMS-Bordeaux (FR)
- ISEN Lille (FR)
- Univ. Wuppertal (DE)
- LETI / CEA Grenoble (FR)
- Delft Univ. of Technology (NL)
- SP Devices AB, (SE)
- Acreo AB, (SE)
- Ericsson AB, (SE)



Designs Fabricated in 2010



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

- **30 designs** have been fabricated in 65nm SOI in **2010**.
- From **7 customers** :

North America (1)

- Stanford University (USA)

Europe (6)

- IMS-Bordeaux (FR)
- IEMN (ISEN) Lille (FR)
- LETI / CEA Grenoble (FR)
- Delft Univ. of Technology (NL)
- Acreo AB, (SE)
- Ericsson AB, (SE)



130nm CMOS SOI Process



Chapitre
Français



Section
France

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H9

C65

C40

C65 SOI

H9 SOI

B9 MW

HCMOS9-SOI Process Features:

- 1 thick oxide for 2.5V power supply
- 6 metal layers
- RF-MOS, RF-PADS, varactors, inductors...
- MPW runs are common to every HCMOS9 bulk (4 MPW runs in 2011)



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Français



Section
France

STMicroelectronics MPW Results 2010



Summary Results 2010



H9

C65

C40

C65 SOI

H9 SOI

B9 MW

12 MPWs, 162 circuits

- HCMOS9GP: 5 MPWs, 46 circuits, 211 mm²
- CMOS065: 3 MPWs, 57 circuits, 148 mm²
- CMOS065-SOI: 2 MPWs, 30 circuits, 99 mm²
- BiCMOS9MW: 2 MPWs, 29 circuits, 274 mm²



Conclusion



- **Excellent Partnership CMP / STMicroelectronics.**
- **Efficient Technical Support**
- **65nm SOI and 130nm SiGe adopted rapidly.**