



CNRS – INPG – UJF

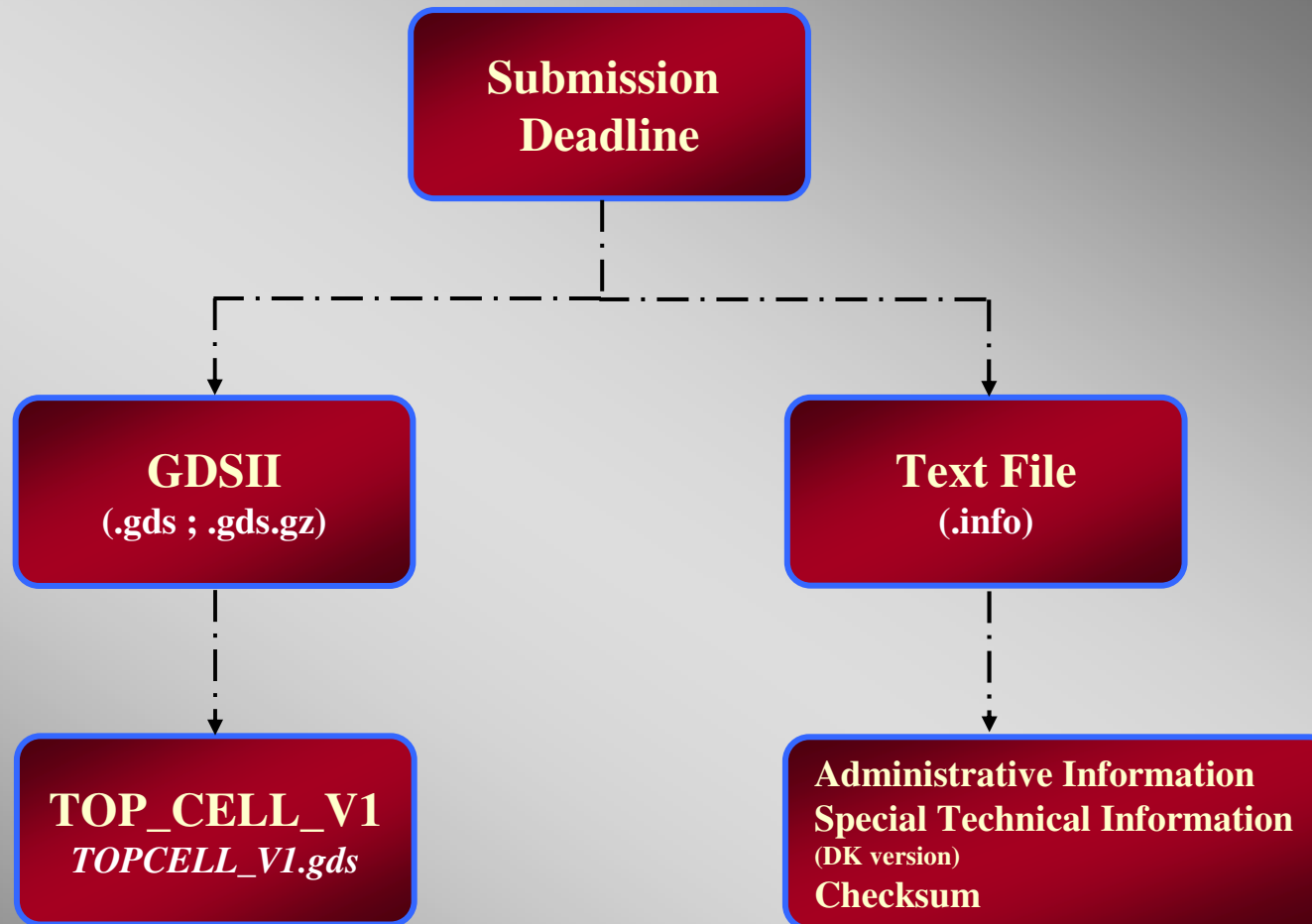
CMP Checks before manufacturing



Submission Rules

DRC tools

Critical errors



△ Do Not use standard cell names for your customs cells △

→ Rename your own cell like MY_INV1 ; MY_NAND20



→ Austriamicrosystems

C35, S35 (0.35 μ): Assura, Calibre, Diva, Tanner (provided by CMP)

C35 bulk micromachining: Diva , Assura

H35 (0.35 μ): Assura, Calibre

→ STMicroelectronics

HCMOS9 (130n): Calibre, Diva & Assura (provided by CMP)

CMOS065 (65n): Calibre

CMOS040 (40n): Calibre

B9MW (130n BiCMOS): Calibre

→ MEMSCAP

PolyMUMPS, MetalMUMPS, SOIMUMPS: Diva, Tanner, Mentor

→ SANDIA

SUMMiT V: Tanner, AutoCad, Cadence (on request)



DRC Interactive interface into Virtuoso



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The screenshot shows the Virtuoso Layout Editing interface. The menu bar includes: Tools, Design, Window, Create, Edit, **Verify**, Connectivity, Options, Routing, **Assura**, Migrate, HIT-KIT Utilities, **Calibre**, and Help. The Verify menu is open, listing options such as MSPS Check Pins..., DRC..., Extract..., Substrate Coupling Analysis..., ConcIc..., ERC..., LVS..., Shorts..., Probe..., and Markers. The Assura menu is also open, listing options like Open Run..., Open Cell..., Technology..., Rule Sets..., Setup, Run DRC..., Run aLPSM..., Run LVS..., Open ELW, Open VLW, LVS Debug Env..., View Netlist..., LVS Error Report..., Probing..., Short Locator..., Run RCX..., and Close Run. The Calibre menu is open, listing options like Run DRC, Run LVS, Run PEX, Start RVE, Clear Highlights, Setup, and About... The main workspace displays a complex PCB layout with various components and routing paths. The status bar at the bottom shows: mouse L: mouseSingleSelectPt, M: leHiMousePopUp(), R: hiRedraw(), and HIT-Kit: 3.70.



Critical errors



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- **Antenna errors**

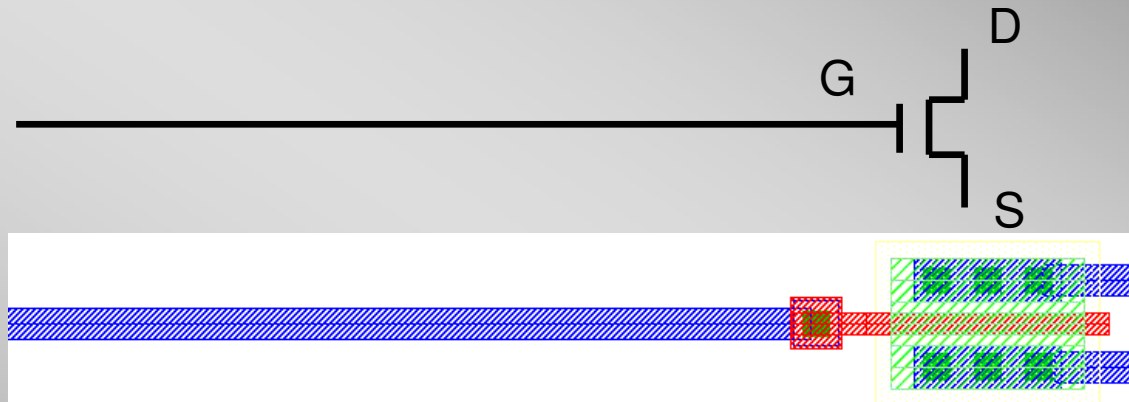
- **Wide-Metal / Metal slots**

- **Density rules**

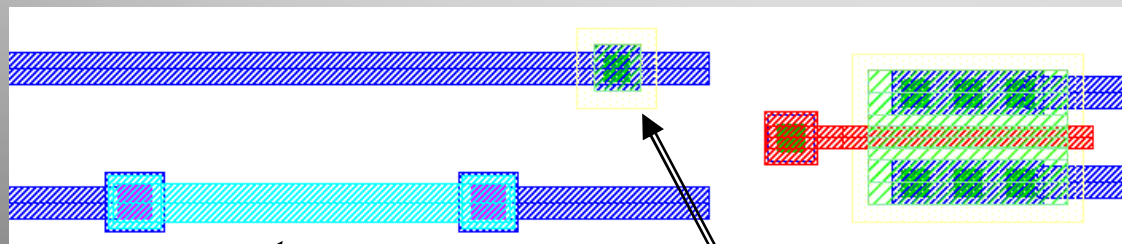
- **Substrate / Wells connections**

→ Problem during the fabrication

There is a maximum ratio to be respected: $\frac{\text{Connection surface}}{\text{Gates surface}}$



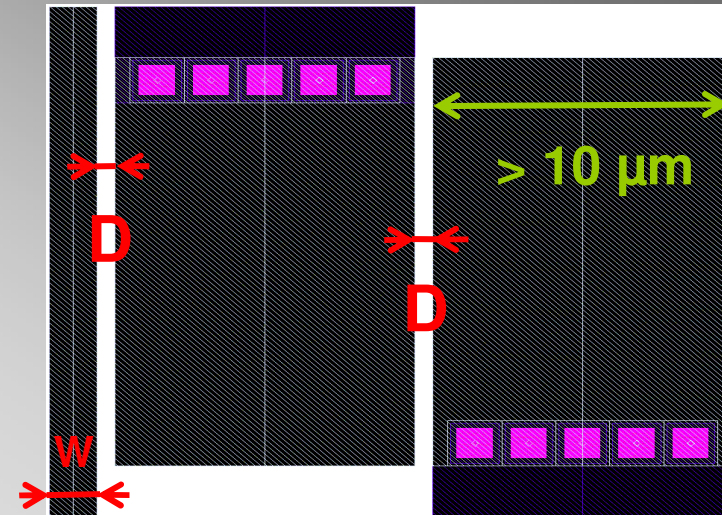
→ 2 possible corrections



1st solution:
upper metal layer bridge

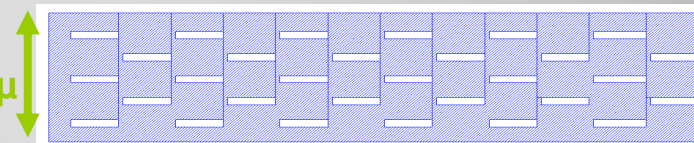
2nd solution:
N+diff / Substrate diode

MET to WIDE MET Spacing



Make openings in the wide metal

$W > 10 \mu$

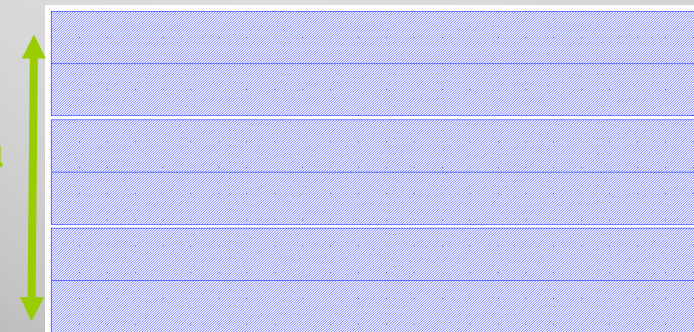


Staggered "metal slot"

Increase the metal and resin adherence

Decrease the electro-migration effects

$W > 10 \mu$

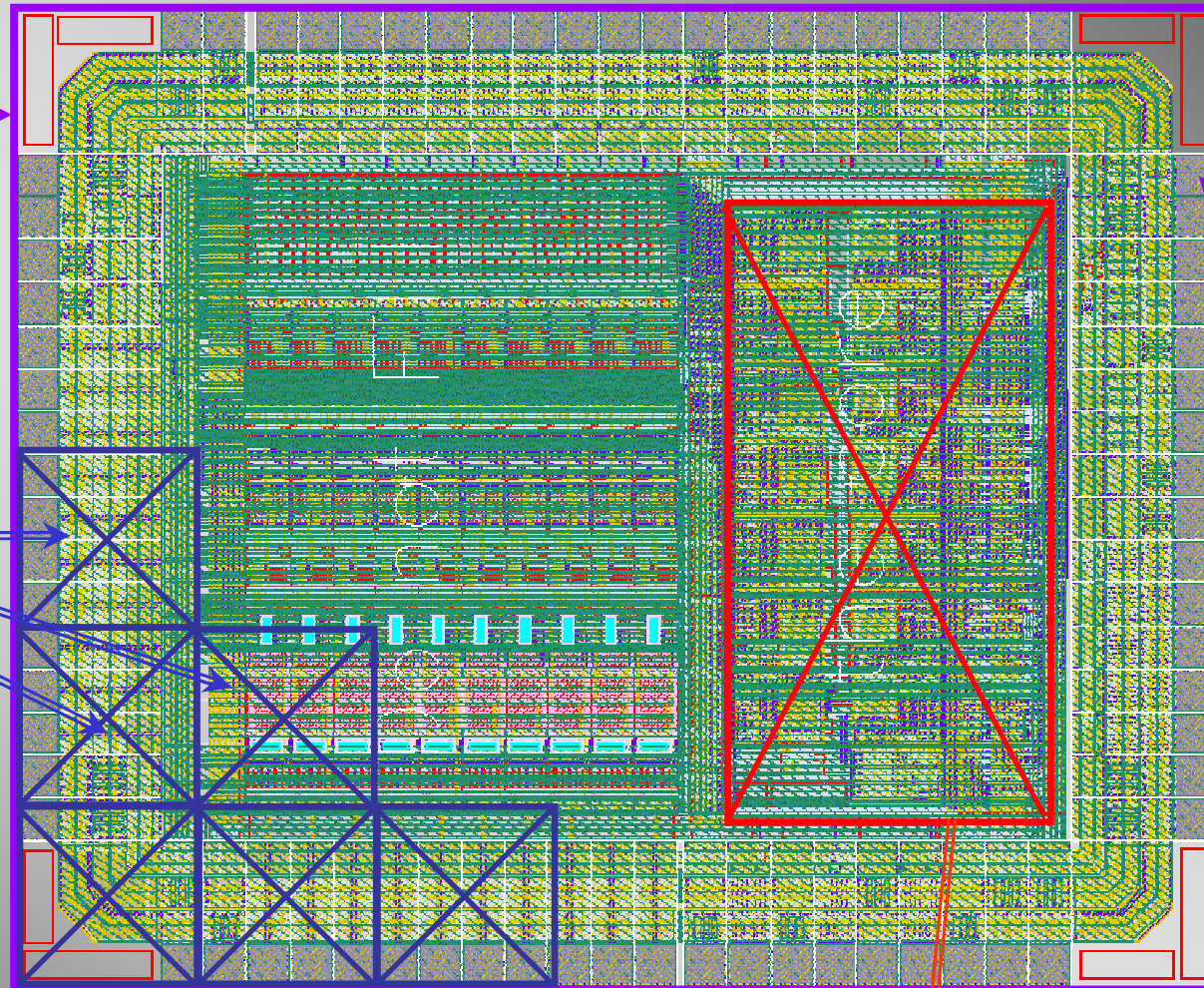


Divide in smaller paths

Full Chip
Verification



Local area
verification



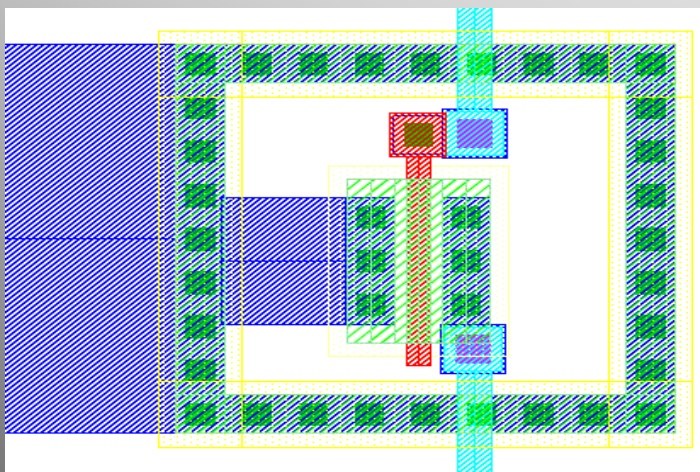
Pad opening
in 65nm

Too large "No Filler" area

→ Polarization contact for NMOSes and PMOSes

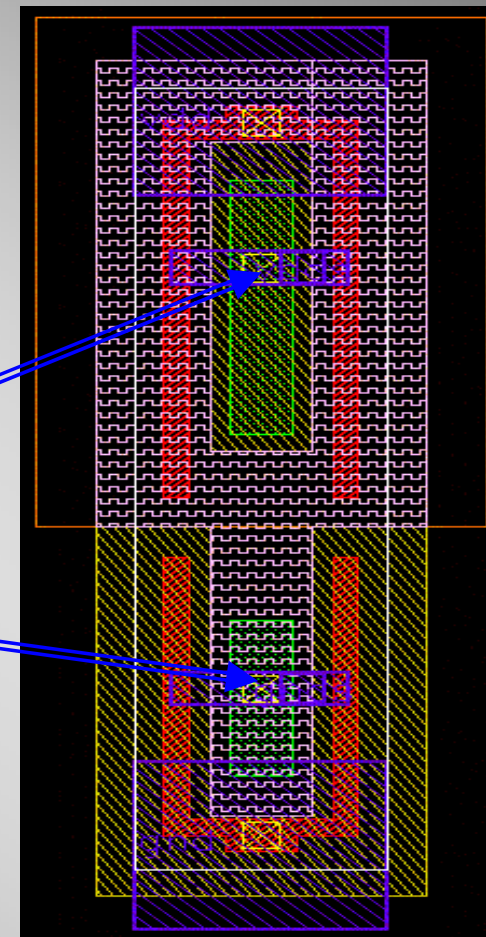
- Must be placed every 25/50 μm
- Recommended to use standard filler cells with polarization contact for the automatic Place & Route with ST 65n and ST 45n processes.

Recommended for full custom



NWell Tap

Substrate Tap



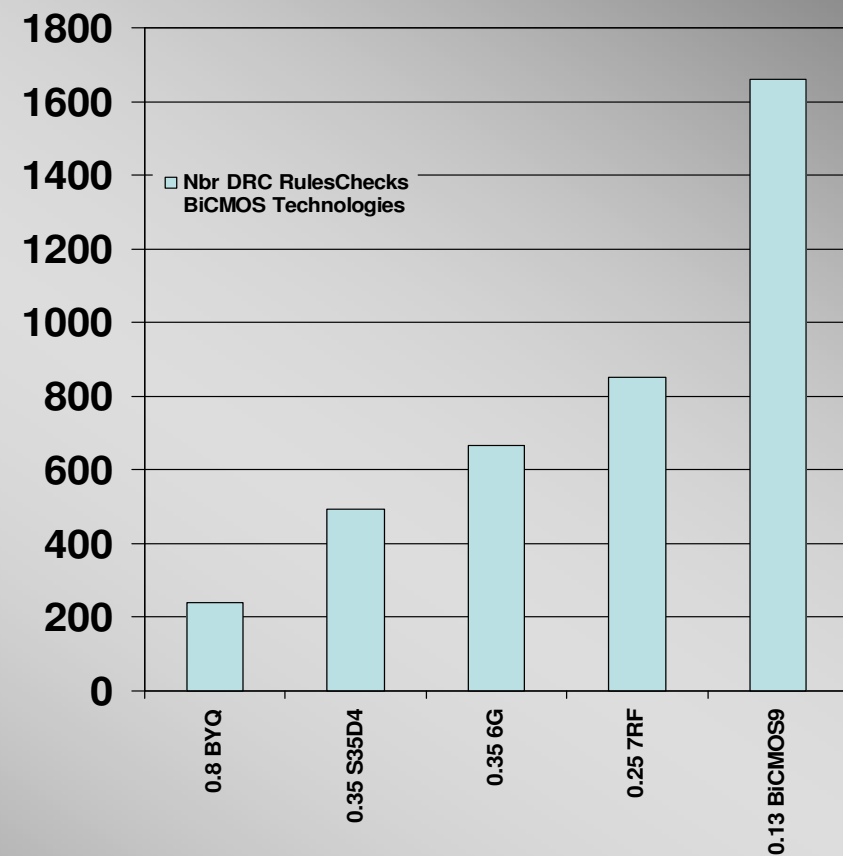
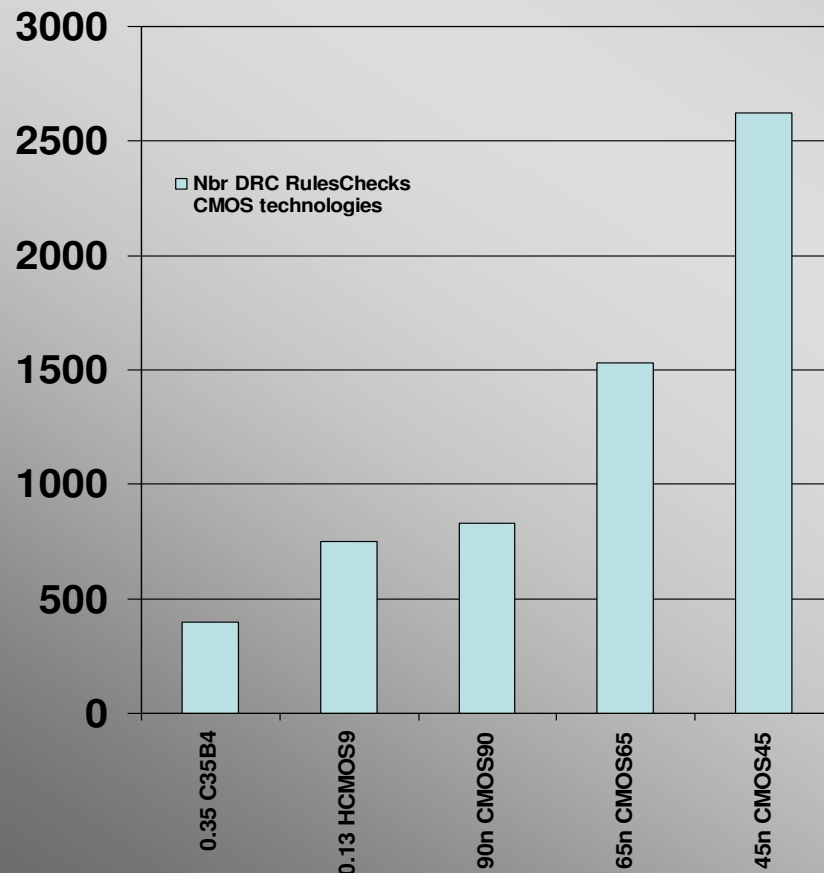


Number of DRC RuleChecks



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Technology & Process	0.35 CMOS C35B4	0.12 CMOS HCMOS9	90 nm CMOS CMOS90	65 nm CMOS CMOS65	45 nm CMOS CMOS45	0.8 BiCMOS BYQ	0.35 SiGe S35D4	0.35 BiCMOS BiCMOS6G	0.25 BiCMOS BiCMOS7RF	0.13 BiCMOS
Nbr. of DRC RuleChecks	400	750	830	1530	2620	240	495	665	850	1660





CMP send the DRC report in different format (Cadence, Mentor Graphics, Tanner . . .)

CMP users correct the design, if needed

CMP ask for approval of the new DRC report.