



CNRS – INPG – UJF



Chapitre
Français



Section
France

Design-Kits, Libraries & IPs



austriamicrosystems

- Supported CAD tools
- Design-kits overview
- Digital, Analog, and RF Libraries
- IPs



STMicroelectronics

- Supported CAD tools
- Design-kits overview
- ST 65nm Tanner PDK
- Standard cell Libraries
- IPs





austriamicrosystems

- **0.35 μ m CMOS**
- **0.35 μ m SiGe**
- **0.35 μ m HV-CMOS**



austriamicrosystems Supported CAD Tools



Chapitre
Français



Section
France

CNRS - INPG - UJF

	Schematic & Design Entry	Electrical Simulation	Digital Simulation	Logic Synthesis	Layout & Verification	P&R
Cadence	Composer (CDS)	Spectre (CDS) Hspice Ultrasim	NC-Sim, AMS-Designer Verilog	BuildGates	Virtuoso-XL Diva Assura	SOC Encounter ICC Silicon Ensemble
Mentor	DA (MGC)	Eldo (MGC)	ModelSim	Leonardo	IC / Calibre	IC-Route
Synopsys	Design Compiler	Hspice	VSS / VCS	Design Compiler	StarRCXT	Astro
Tanner	S-Edit	TSpice	TSpice	---	L-Edit DRC	SPR
		Pspice (CDS)				
		Saber (Synopsys)				
		ADS (Agilent)				
		Smash (Dolphin)				
		SmartSpice (Silvaco)				



● Current distributions :

	Cadence (SUN / HP / Linux)		Mentor (SUN / Linux)	Tanner (MS-Windows)
	CDB	OA		
0.35μm CMOS	3.70	4.0	3.70	7.2
0.35μm SiGe	3.70	4.0	3.70	
0.35μm HV-CMOS	3.72	4.0	3.71	



LV Digital standard cells and IO Libraries :

CORELIB : General purpose digital library

CORELIB_3B : Same as CORELIB with 3 busses (VDD, VSS, GND)

IOLIB : IO pads (input, output, bidir). 3.3V and 5V available

IOLIBC_3B : Core limited digital IO Libraries



Core and IO cells are characterized for 1.8V, 2.2V, 2.7V, 3.3V.

HV Digital standard cells and IO Libraries :

CORELIB_HV : CORELIB for high voltage.

IOLIB_HV : High Voltage digital IO pads library

Analog standard cells Libraries :

IOLIB_ANA : Analog IO pads library

IOLIBC_ANA_3B : Core limited Analog IO pads library

IOLIB_ANA_HV : High Voltage Analog IO pads library



A_CELLS : Analog Library

RF standard IO cells Libraries :

SPIRAL : Library with characterized Inductors

RF_PADS : RF IO pads library



IP blocks available from CMP free of charge to Univ. & Research (0.35µ CMOS)

Single & Dual Port RAMS configurations:

Words \ Bits	8	9	12	16	32
128	SP	SP	SP	SP	SP
256	DP			SP / DP	SP
512				SP	SP
600				SP	
1024	SP / DP			SP / DP	
2048	SP			SP / DP	SP
4098	DP				

austriamicrosystems

Generate a Memory Simulation Model

For more information about memory blocks and possible configurations please take a look at [Digital Macros & Blocks](#)

Please contact your local sales representative to order the generation of the final memory layout data.

Before you start, please check your [Profile](#)

Please specify your memory

Process: C35
 Metalization: Triple Metal
 Voltage: 3.3V
 Model: Single Port RAM
 Data Bus: Separated Inputs and Outputs
 Number of Words:
 Number of Bits/Word:

Estimate Reset

Single Port RAM
 Dual Port RAM
 Diffusion ROM



STMicroelectronics

- **HCMOS9** (*130nm CMOS*)
- **HCMOS9-SOI** (*130nm CMOS-SOI*)
- **BiCMOS9-MW** (*130nm CMOS*)
- **CMOS065** (*65nm CMOS*)
- **CMOS065-SOI** (*65nm CMOS-SOI*)
- **CMOS040** (*40nm CMOS*)



STMicroelectronics supported CAD Tools



Chapitre
Français




Section
France

CNRS – INPG – UJF

	IC		Electrical Simulation				Verification	Parasitics Extraction			P&R	
	CDB 5.1.41	OA 6.1.4	Spectre (CDS)	Eldo (MGC)	Hspice (SNPS)	ADS (Agilent)	Calibre (MGC)	StarRCXT (SNPS)	Calibre (MGC)	QRC (CDS)	Encounter (CDS)	ICC (SNPS)
HCMOS9	X		X	X	X		X	X			X	X
HCMOS9- SOI	X		X	X		X	X	X	X		-	-
BiCMOS9- MW	X		X	X	X	X	X	X	X			X
CMOS065	X	X	X	X	X	X	X	X	X		X	X
CMOS065- SOI	X		X	X			X	X				X
CMOS040		X	X				X			X	X	X



● Current distributions :

	Cadence (SUN / HP / Linux)	Tanner (MS-Windows)
HCMOS9	9.2	
HCMOS9-SOI	9.7	
BICMOS9-MW	2.2	
CMOS065	5.3.4	V3 
CMOS065-SOI	4.2	
CMOS040	2.1	

- RF option available for HCMOS9 & CMOS065 design kits.



ST 65nm Tanner PDK



● Full-Custom design environment (Frontend + Backend)

All basic devices have been ported from the ST environment to the Tanner Tools

Frontend :

- Schematic Capture using S-Edit.
- Spice simulation using TSpice.

Backend :

- Layout Edition using L-Edit.
- Verification using L-Edit/DRC and LVS.

● To be done :

- Parametric layout cells (T-Cells)
- Standard-cells (schematics and abstracts)
- Qualifying the HiPer Design Suite



● CORE cells Libraries :

- CORE : General purpose core libraries
- CORX : Complementary core libraries (complex gates)
- CLOCK : Buffer cells and the same for clock tree synthesis
- PR : Place and route filler cells and the same.
- DP : Datapath leaf cells libraries
- HD : High density core libraries

} on request

● IO cells Libraries :

1.8V, 2.5V, 3.3V IO pads:

- 80 μ , 65 μ , 60 μ , 50 μ 40 μ and 30 μ IO pads : Digital and Analog
- Staggered IO pads
- Flip-Chip pads
- Level Shifters, and compensation cells

On request:

- LVDS Pads
- DLL, PLL
- ...

● Memories SPRAM / DPRAM / MPRAM / ROM available on request, *free of charge* (1-2 weeks delay)



IP Blocks Available from STMicroelectronics



- **ARM 946EJ-S :**

 - HCMOS9 130nm CMOS IP core

 - Simulation models

 - Abstract view for P&R

 - Timing Files for STA and backannotated simulation

 - Available under NDA

- **ARM 926EJ-S :**

 - CMOS065 65nm CMOS IP core

 - Simulation models

 - Abstract view for P&R

 - Timing Files for STA and backannotated simulation

 - Available under NDA

+ Access to all available ARM cores in 65nm.



CNRS – INPG – UJF

Design-Kit Support at CMP



Chapitre
Français



Section
France

- Management and support of the DK distribution and updates.
- Development, support and maintenance of design-kits.
- Tutorials on some design flows.
- Two CMP engineers working partly at ST to solve all kind of support with ST design-kits and memory blocks generation.