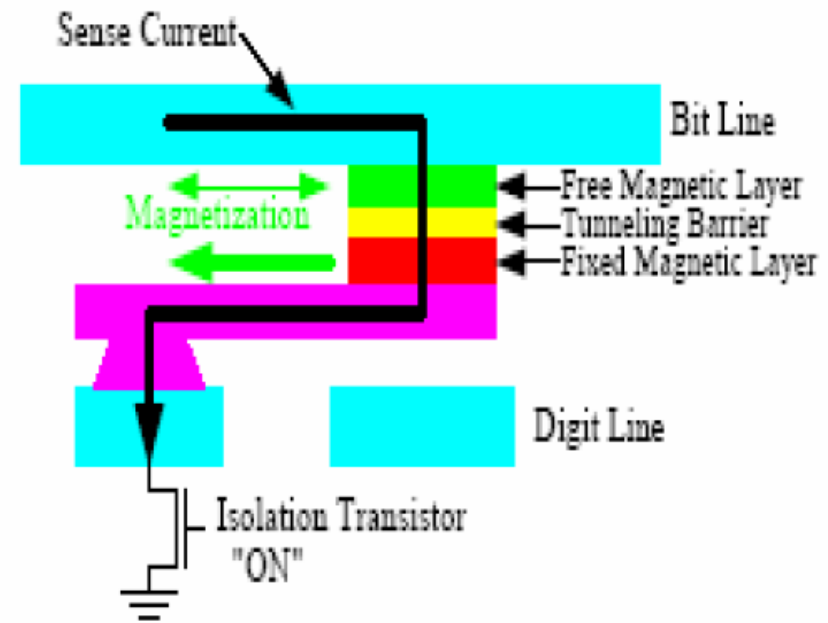
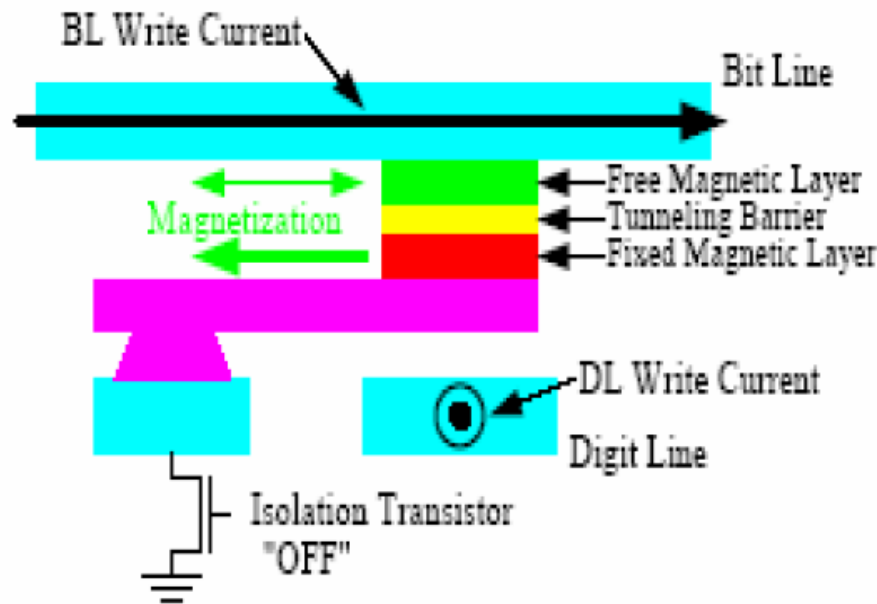
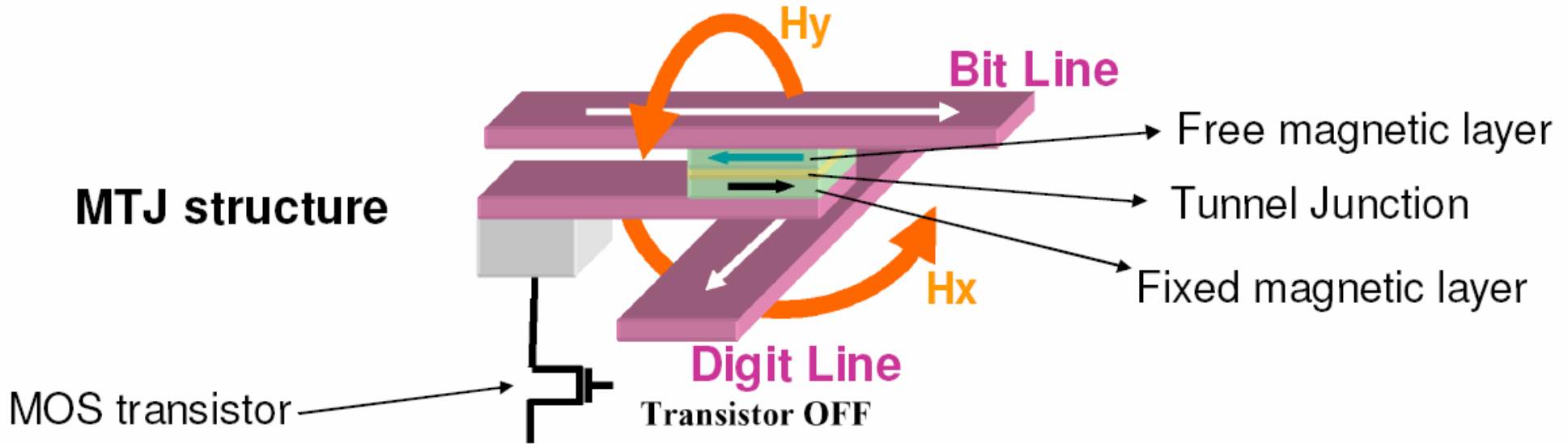


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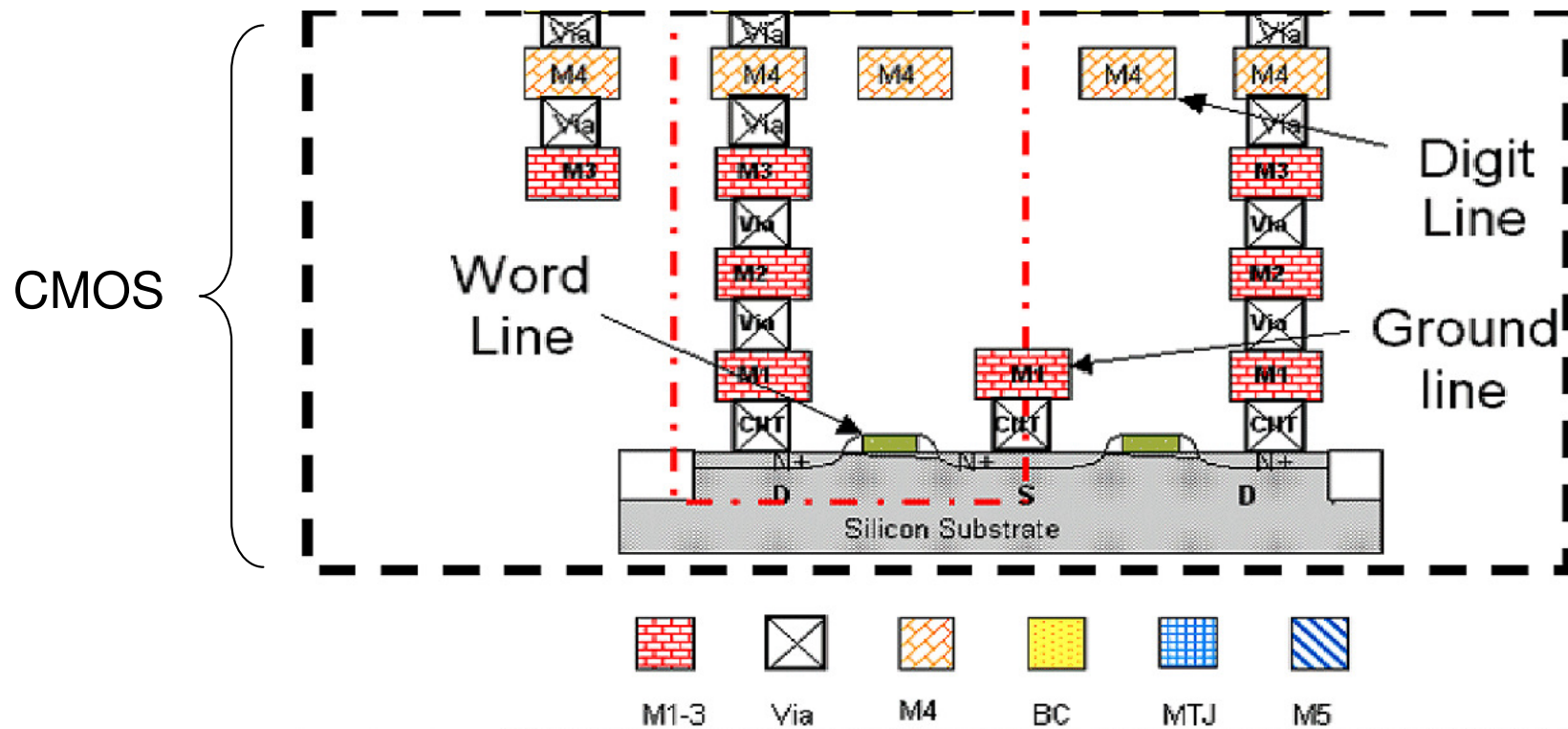
CMOS - Magnetic Integration

Developments and results at CMP

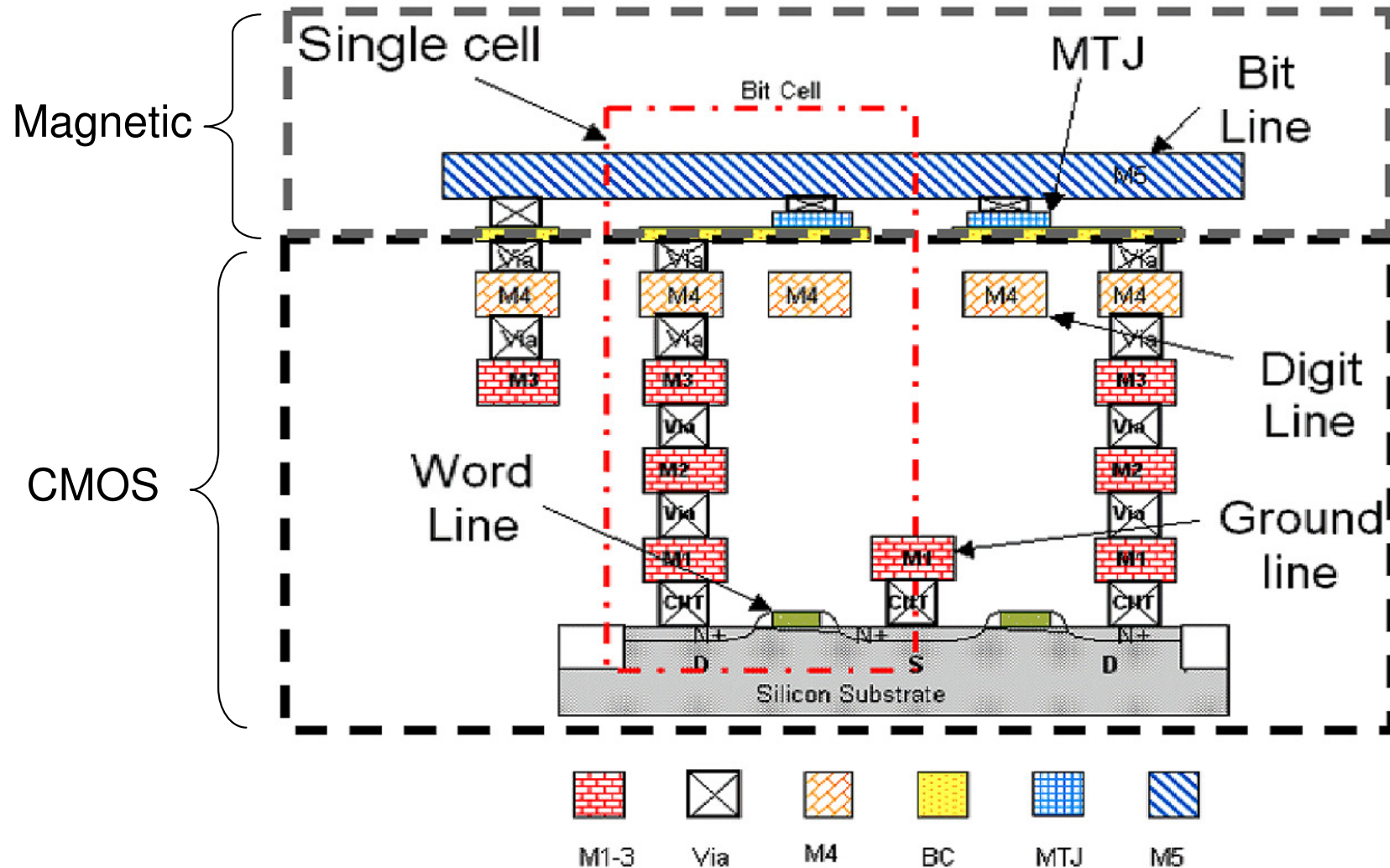
MTJ structure



- CMOS process done at the foundry (stop at the top metal layer)



- CMOS process done at the foundry (stop at the top metal layer)
- Magnetic post-process + metallization + passivation + pad openings





MTJ above-IC on CMOS process



CNRS - INPG - UJF

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ANR **CILOMAG Consortium**

Silicon Foundries

MTJ Postprocess



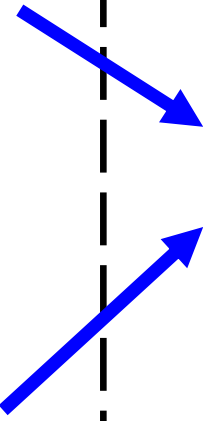
ae *austriamicrosystems*

0.35 μ

ST STMicroelectronics

130nm, (90nm)

cea **leti**

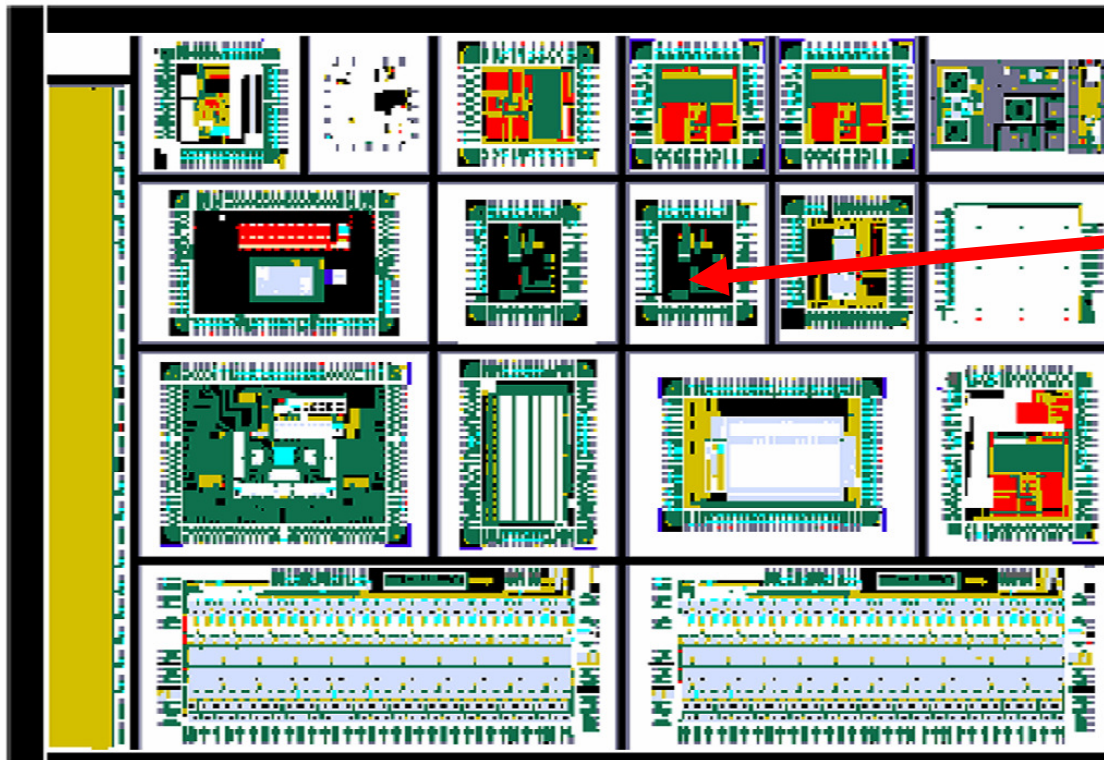




- **Collect the process information : design-rules, MTJ models**
- **Build the design-kit as an add-on on the standard foundry DK**
- **Distribute the DK to the partners with technical support**
- **Organize the reticle with design collections from the partners**
- **Interface with the foundry with the few process stop constraints**
- **Interface with the post-process (technical and logistics)**
- **Organize the sawing and packaging**

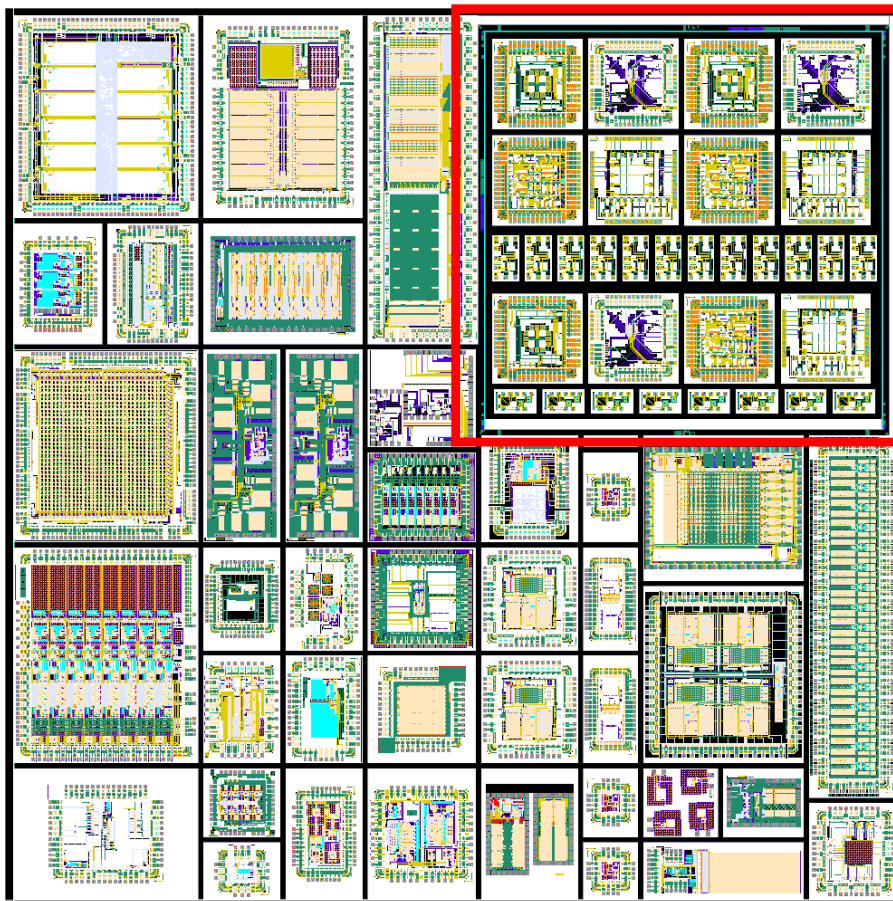
One of the project's goal : Enable the access to CMOS-MTJ from CMP.

- Designer : LIRMM (Montpellier)
- Application : Non Volatile FPGA prototype.
- CMOS process : Austriamicrosystems 0.35um CMOS
- CMP MPW run : A35C7-2
- Magnetic Post-Process : INESC (Portugal)



First CMOS MRAM Prototypes
ever made in a MPW run

- Designers : All CILOMAG partners
- Application : Different blocks architectures.
- CMOS process : Austriamicrosystems 0.35um CMOS
- CMP MPW run : A35C8-2
- Magnetic Post-Process : LIMN / LETI (Grenoble) Delivery : Q1 2010

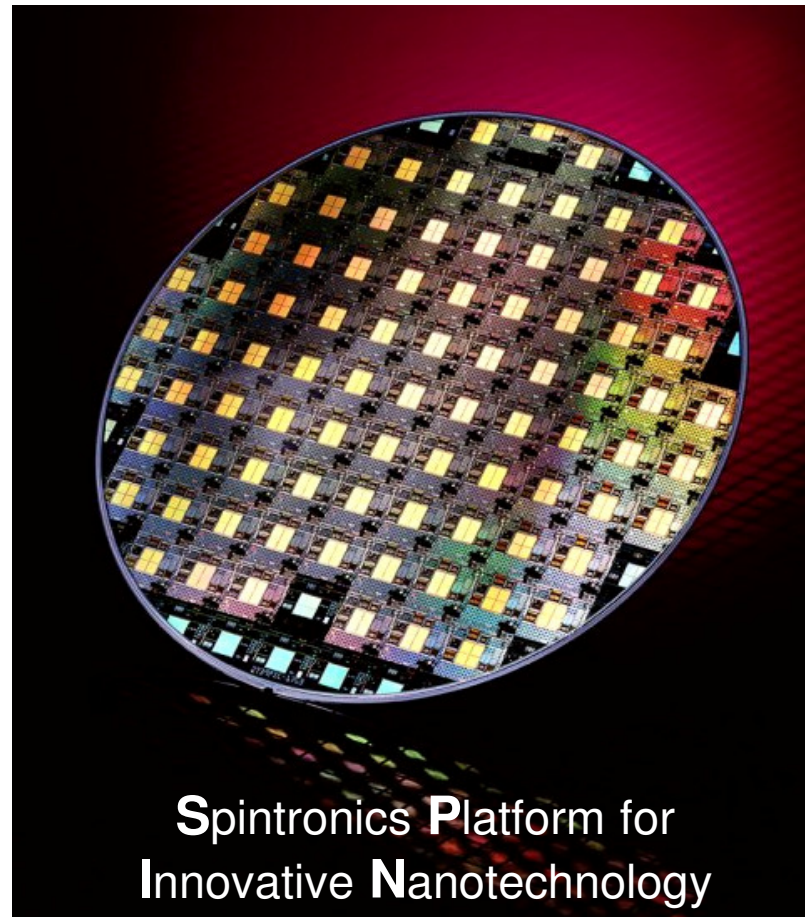


Embedded CMOS MTJ MPW
in a CMOS MPW

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ANR

SPIN



11 partners



Démonstrateur 1
Filière Spin-valve

Capteurs pour la
Santé et l'électronique
de puissance

Technologie BE
>250nm

Spintronics Platform for
Innovative Nanotechnologies

- Conception / design (Plateforme Saclay)
- Layout / assemblage / gestion MPW
- FE CMOS
- BE magnétique (Plateforme Grenoble)
- Packaging

Démonstrateur 2
Filière JTM

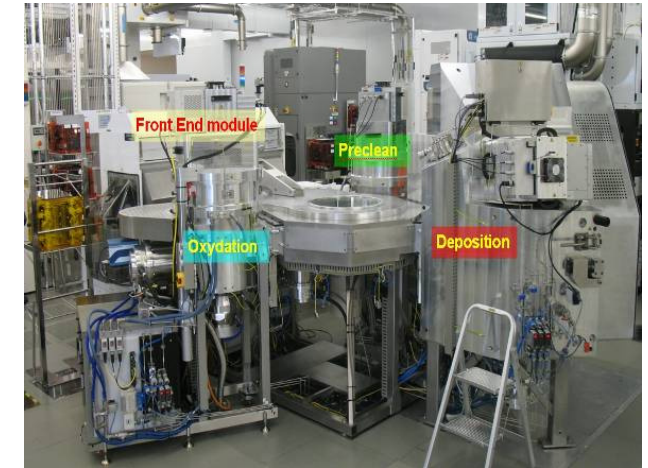
Système de calcul
basse consommation

Technologie BE
≤120nm



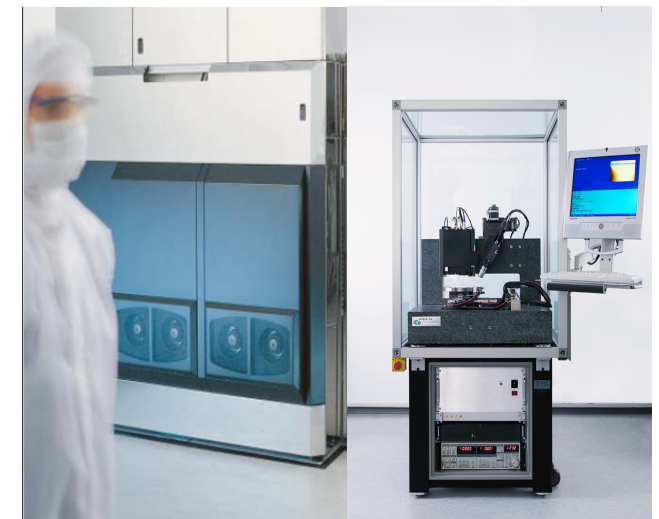
LIRMM
SPEC
LIST
LETI-DCIS
MENTA

Design Sensor / Logic
+ ASIC design for Sensors



SPINTEC
IEF
CMP
CROCUS

Magnetic Process Design Kit
Digital PDK+ PDK for sensors



LETI/DIHS
LTM

Ligne BE magnétique
+ Dépôt 200mm IBS AVIZA
+ Carac magnéto-transport CAPRES
+ Four de recuit 200mm
+ Gravure RIE pour Spintronique



- **Designers : All ANR-SPIN partners**
- **Application : Different blocks architectures (FPGA, Latch, etc ...).**
- **CMP embedded the Magnetic PDK into the ST design-kit**
- **CMOS process : STMicroelectronics 130nm CMOS**
- **CMP MPW run : S13C9-4 (September 2009)**
- **Magnetic Post-Process : LIMN / LETI (Grenoble) Delivery : Q2 2011**



- ❑ **Crocus magnetic post-process is fully qualified on TowerJazz 130nm CMOS**
- ❑ **A complete Hybrid CMOS/Magnetic design-kit exists.**
- ❑ **CMP is discussing with TowerJazz to offer the process in 2011.**