Technology Processes & Runs in 2013

http://cmp.imag.fr
0.35\(\mu\) Process Presentation:
- CMOS
- CMOS-Opto
- SiGe
- HV-CMOS
- HV-CMOS EEPROM/Flash

0.18\(\mu\)m HV-CMOS, and CMOS

Activity in 2013

HRES wafers / DRIE trenching / 50\(\mu\)m Wafer thinning
IPHC / LBNL / STAR Experiment

Nipson Technology

Conclusion
Available Processes

C18A6 : 0.18µ CMOS

H18A6 : 0.18µ HV-CMOS

C35B4C2 : 0.35µ CMOS 3.3V

C35B4C3 : 0.35µ CMOS 3.3V / 5.0V

C35B4O1 : 0.35µ CMOS-Opto

S35D4M5 : 0.35µ SiGe

C35B4M3 : 0.35µ CMOS-RF

H35B4D3 : 0.35µ HV-CMOS

H35B4H3 : 0.35µ HV EEPROM

0.8µ BiCMOS : BYE / BYQ (Engineering runs available)
0.6µ CMOS (Engineering runs available)
0.35μ CMOS
CMOS 0.35 µ C35 (C35B4C3)

- 2 Layers Polysilicon, 4 Layers Metal, 3.3V / 5.0V, High Resistive Poly.
- 3.3V / 5.0V I/O pads.
- Peripheral cells with high driving capability (from 1mA to 24mA)
- Application: Analog, Digital, Mixed A/D, RF.
- Density: 18 kgates/mm²
- Gate Delay: 100ps (NAND2 typical)

- CORELIB qualified for 1.8V / 2.2V / 2.7V / 3.3V
- CORELIB_V5 qualified for 2.0V / 3.0V / 4.0V / 5.0V

CMP annual users meeting, 23 January 2014, PARIS
CMOS 0.35 µ **C35 (C35B4C2)**

- 2 Levels Polysilicon, 4 Levels Metal, **3.3V only**, High Resistive Poly.
- **3.3V** I/O pads.
- Peripheral cells with high driving capability (from 1mA to 24mA)
- Application: Analog, Digital, Mixed A/D, RF.
- Density: 18 kgates/mm²
- Gate Delay: 100ps (NAND2 typical)
- Digital Libraries qualified for 1.8V / 2.2V / 2.7V / 3.3V
Thick Metal and MIM available in C35B4M3.
## CMOS 0.35µ C35 Features

<table>
<thead>
<tr>
<th>Process Name</th>
<th>units</th>
<th>C35B3C0</th>
<th>C35B3C1</th>
<th>C35B4C2</th>
<th>C35B4C3</th>
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<tbody>
<tr>
<td><strong>Process Type</strong></td>
<td></td>
<td>mixed signal CMOS</td>
<td>mixed signal CMOS</td>
<td>mixed signal CMOS</td>
<td>mixed signal CMOS</td>
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<tr>
<td><strong>Drawn MOS Channel Length</strong></td>
<td>µm</td>
<td>0.35</td>
<td>0.35</td>
<td>0.35</td>
<td>0.35</td>
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<tr>
<td><strong>Operating Voltage</strong></td>
<td>V</td>
<td>2.5 - 3.6</td>
<td>3.3V / 5.0V</td>
<td>3.3 V</td>
<td>3.3V / 5.0V</td>
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<td><strong>Number of Masks</strong></td>
<td></td>
<td>14</td>
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<td><strong>Number of Masking layers</strong></td>
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<td><strong>Number of Metal Layers</strong></td>
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<tr>
<td><strong>Number of Poly Layers</strong></td>
<td></td>
<td>2</td>
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<tr>
<td><strong>Substrate Type</strong></td>
<td></td>
<td>p</td>
<td>p</td>
<td>p</td>
<td>p</td>
</tr>
<tr>
<td><strong>Diffusion Pitch</strong></td>
<td>µm</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td><strong>Metal1/2/3/4 Pitch</strong></td>
<td>µm</td>
<td>0.95 / 1.1 / 1.1 / 1.2</td>
<td>0.95 / 1.1 / 1.1 / 1.2</td>
<td>0.95 / 1.1 / 1.1 / 1.2</td>
<td>0.95 / 1.1 / 1.1 / 1.2</td>
</tr>
<tr>
<td><strong>Metal1/2/3/4 conacted Pitch</strong></td>
<td>µm</td>
<td>1.05 / 1.2 / 1.2 / 1.3</td>
<td>1.05 / 1.2 / 1.2 / 1.3</td>
<td>1.05 / 1.2 / 1.2 / 1.3</td>
<td>1.05 / 1.2 / 1.2 / 1.3</td>
</tr>
<tr>
<td><strong>Poly1 Pitch</strong></td>
<td>µm</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
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<tr>
<td><strong>High Resistive Poly</strong></td>
<td>kOhm/#</td>
<td>-</td>
<td>-</td>
<td>1,2</td>
<td>1,2</td>
</tr>
<tr>
<td><strong>Poly1/Poly2 Precision Caps</strong></td>
<td>fF/µm²</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td><strong>N/PMOS Channel Length</strong></td>
<td>µm</td>
<td>0.30/0.30</td>
<td>0.30/0.30</td>
<td>0.30/0.30</td>
<td>0.30/0.30</td>
</tr>
<tr>
<td><strong>N/PMOS Saturation Current</strong></td>
<td>µA/µm</td>
<td>520 / 240</td>
<td>520 / 240</td>
<td>520 / 240</td>
<td>520 / 240</td>
</tr>
<tr>
<td><strong>Flip-Flop Delay</strong></td>
<td>ns</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
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<tr>
<td>*<em>NAND2 Delay <em>)</em></em></td>
<td>ns</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
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<tr>
<td><strong>NAND2 Area</strong></td>
<td>µm²</td>
<td>54.6</td>
<td>54.6</td>
<td>54.6</td>
<td>54.6</td>
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<tr>
<td><strong>NAND2 Power</strong></td>
<td>µW/MHz</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>
0.35µ CMOS-Opto
CMOS-Opto 0.35 µ (C35B401)

- Planarization and anti-reflective coating allows better optical features.
- P-Epi wafers for lowering current leakage in the diode (lower dark current).

C35-Opto Process Cross-Section
CMOS-Opto 0.35 µ (C35B4O1)
(100% compatible with standard 4LM 0.35µ CMOS)

Process features:
• 0.35 µ CMOS polycide-gate process
• 4 layers metal and 2 layers poly
• Peripheral Cells with high driving capabilities (1mA – 24mA)
• High performance digital and mixed signal capabilities
• N/PMOS saturation current : 520/240 µA/µm

Opto features:
• Dark current < 45 pA/cm²
• Cut-off frequency > 20 MHz
• Responsitivity @ 550 nm: 290 mA/W
• Responsitivity @ 850 nm: 330 mA/W
• Cut-off frequency of photodiode: 20 MHz

Applications:
Photo sensors, APS, CMOS Camera ...

Responsitivity Curve of Photodiode
(Courtesy AMS AG)
CMOS-Opto 0.35 µ

- Design-rules and Electrical Parameters compatible with the C35 standard process. **(HRES is available only in MPW runs)**

- Design-kit compatible with the 4 layers metal process option C35B4.

- Every C35 MPW run planned by CMP includes the CMOS-Opto option.

- 5 MPW runs scheduled in 2014.

- MPW Price : 810 Euro/mm² (minimum price 3 mm²)
0.35µ SiGe
SiGe HBT-BiCMOS 0.35 μ S35

- 4 Layers Polysilicon / 4 Layers Metal.
- Power supply voltage range (2.5V – 3.6V / 5.5V)
- Vertical SiGe-HBT NPN : $F_t = 70$ GHz
- High Resistive Polysilicon.
- High precision Poly1/Poly2 capacitors
- High precision MIM capacitors
- Thick Top Metal
### SiGe HBT BiCMOS 0.35 µm S35 (S35D4M5)

- 4 Levels Polysilicon, 4 Levels Metal, 3.3V / 5.0V, High Resistive Poly, Thick Metal, MIM capacitors.

<table>
<thead>
<tr>
<th>Process Name</th>
<th>units</th>
<th>S35D3M2</th>
<th>S35D4M2</th>
<th>S35D4M5</th>
</tr>
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<tbody>
<tr>
<td><strong>Process Type</strong></td>
<td></td>
<td>SiGe-BiCMOS</td>
<td>SiGe-BiCMOS</td>
<td>SiGe-BiCMOS</td>
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<tr>
<td><strong>Drawn MOS Channel Length, Drawn Emitter Width</strong></td>
<td>µm</td>
<td>0.35</td>
<td>0.35</td>
<td>0.35</td>
</tr>
<tr>
<td></td>
<td>µm</td>
<td>0.40</td>
<td>0.40</td>
<td>0.40</td>
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<tr>
<td><strong>Operating Voltage CMOS</strong></td>
<td>V</td>
<td>2.5-3.6</td>
<td>2.5-3.6</td>
<td>2.5-3.6 / 5.5</td>
</tr>
<tr>
<td><strong>Number of Metal Layers</strong></td>
<td></td>
<td>3</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td><strong>Number of Poly Layers</strong></td>
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<td>4</td>
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<tr>
<td><strong>Substrate Type</strong></td>
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<td>p</td>
<td>p</td>
<td>p</td>
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<tr>
<td><strong>Diffusion Pitch</strong></td>
<td>µm</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td><strong>Metal1/2/3 Pitch</strong></td>
<td>µm</td>
<td>0.95/1.1/1.2</td>
<td>0.95/1.1/1.2</td>
<td>0.95/1.1/1.2</td>
</tr>
<tr>
<td><strong>Poly1 Pitch</strong></td>
<td>µm</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
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<tr>
<td><strong>Thick Metal 4 pitch</strong></td>
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<td>-</td>
<td>4.5</td>
<td>4.5</td>
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<tr>
<td><strong>High Resistive Poly</strong></td>
<td>kOhm/#</td>
<td>-</td>
<td>-</td>
<td>1.2</td>
</tr>
<tr>
<td><strong>Poly1 / Poly2 Precision Caps</strong></td>
<td>fF/µm²</td>
<td>0.9</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td><strong>Metal 2 / Metal 3 Precision Caps</strong></td>
<td>fF/µm²</td>
<td>1.25</td>
<td>1.25</td>
<td>1.25</td>
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<tr>
<td><strong>N/P MOS Active Channel Length</strong></td>
<td>µm</td>
<td>0.3/0.3</td>
<td>0.3/0.3</td>
<td>0.3/0.3</td>
</tr>
<tr>
<td><strong>N/P MOS Saturation Current</strong></td>
<td>µA/µm</td>
<td>540/240</td>
<td>540/240</td>
<td>540/240</td>
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<tr>
<td><strong>Gain</strong></td>
<td></td>
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<td>160</td>
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<tr>
<td><strong>Early Voltage VAF</strong></td>
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<td>100</td>
<td>100</td>
<td>100</td>
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<tr>
<td><strong>HS-HBT: BVceo</strong></td>
<td>V</td>
<td>2.7</td>
<td>2.7</td>
<td>2.7</td>
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<tr>
<td><strong>ft / fmax</strong></td>
<td>GHz</td>
<td>60 / 70</td>
<td>60 / 70</td>
<td>60 / 70</td>
</tr>
<tr>
<td><strong>HV-HBT: BVceo</strong></td>
<td>V</td>
<td>-</td>
<td>-</td>
<td>5.5</td>
</tr>
<tr>
<td><strong>ft / fmax</strong></td>
<td>GHz</td>
<td>-</td>
<td>-</td>
<td>35 / 50</td>
</tr>
</tbody>
</table>
0.35µ HV-CMOS
HV CMOS 0.35 μ **H35 (H35B4D3)**

- 2 Layers Polysilicon, 4 Layers Metal, High Resistive Poly, Thick 4\textsuperscript{th} Metal.

- 20V / 50 V / 120 V Maximum operating voltage.

- 3.3V / 5.0V / 20V Maximum gate voltage.

- $R_{\text{on}} = 0.11 \text{ Ohm mm}^2$ for HV-NMOS
- $R_{\text{on}} = 0.29 \text{ Ohm mm}^2$ for HV-PMOS
HV CMOS 0.35μ Cross Section (H35)

Isolated 3.3V / 5V

Standard 3.3V / 5V

NMOS50 (50V)  PMOS50 (50V)  NMOSI50 (50V)  VERTN1
NMOS120 (120V)  PMOS120 (120V)

CMP annual users meeting, 23 January 2014, PARIS
### High Voltage CMOS 0.35µm H35 Features

<table>
<thead>
<tr>
<th>Process Name</th>
<th>H35B3KC</th>
<th>H35B3LC***</th>
<th>H35B4KD***</th>
<th>H35B4LD***</th>
<th>H35B4D3</th>
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</thead>
<tbody>
<tr>
<td>Number of masks</td>
<td>13</td>
<td>16</td>
<td>19</td>
<td>22</td>
<td>27</td>
</tr>
<tr>
<td>Max. operating voltage HV-NMOS [V]</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50 / 120</td>
</tr>
<tr>
<td>Max. operating voltage HV-PMOS [V]</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50 / 120</td>
</tr>
<tr>
<td>specific R_on* HV-NMOS [Ohm mm²]</td>
<td>0.11</td>
<td>0.11</td>
<td>0.11</td>
<td>0.11</td>
<td>0.11</td>
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<tr>
<td>specific R_on* HV-PMOS [Ohm mm²]</td>
<td>0.29</td>
<td>0.29</td>
<td>0.29</td>
<td>0.29</td>
<td>0.29</td>
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<tr>
<td>Drawn LVMOS Channel Length [µm]</td>
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<td>0.35</td>
<td>0.35</td>
<td>0.35</td>
<td>0.35</td>
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<tr>
<td>Operating voltage LV-MOS [V] **</td>
<td>3.3V, 5V</td>
<td>3.3V, 5V</td>
<td>3.3V, 5V</td>
<td>3.3V, 5V</td>
<td>3.3V, 5V</td>
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<tr>
<td>Max. gate voltage [V]</td>
<td>3.3V, 5V, 20V</td>
<td>3.3V, 5V, 20V</td>
<td>3.3V, 5V, 20V</td>
<td>3.3V, 5V, 20V</td>
<td>3.3V, 5V, 20V</td>
</tr>
</tbody>
</table>

| 2M.....2 metal layers | 3M.....3 metal layers | 4M.....4 metal layers | 1P.....1 poly layer | 2P.....2 poly layers | HP.....high resistive poly | S.....substrate related LV devices | TM.....thick metal layer | 5V.....5V gate oxide | 20V.....20V gate oxide |

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**CMP annual users meeting, 23 January 2014, PARIS**
HV-CMOS 0.35 µ

- LV CMOS fully compatible with C35.
- Design-kits available for Cadence.
- 4 MPW runs scheduled in 2014.
- MPW Price: 1000 Euro/mm² (minimum price 7 mm²)
0.35µ HV-CMOS EEPROM/Flash
HV-CMOS 0.35 µ with Embedded EEPROM / Flash

- HV-CMOS fully compatible with H35.
- EEPROM or Flash available on request.
- Simulation files and abstract view for P&R are accessible. (layout block replacement done at AMS).
- License fees (contact CMP)
- Prototyping price : Contact CMP
Available EEPROM Blocks

<table>
<thead>
<tr>
<th>Process</th>
<th>Block Size</th>
<th>Organization</th>
<th>Read Supply</th>
<th>Write Supply</th>
<th>Endurance</th>
<th>Data Retention</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>H35</td>
<td>64x8 bit</td>
<td>EEPROM</td>
<td>1.8 – 3,6V</td>
<td>1.8 – 3,6 V</td>
<td>80k @ 125°C</td>
<td>&gt;20 years @ 125°C</td>
<td>0.36mm²</td>
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<tr>
<td>H35 (mid-ox only)</td>
<td>128x8 bit</td>
<td>EEPROM</td>
<td>2.3 – 5.5V</td>
<td>2.3 – 5.5 V</td>
<td>80k @ 125°C</td>
<td>&gt;20 years @ 125°C</td>
<td>0.54mm²</td>
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<tr>
<td>H35</td>
<td>1Kx8 bit</td>
<td>EEPROM</td>
<td>2.7 – 3.6 V</td>
<td>2.7 – 3.6 V</td>
<td>80k @ 125°C</td>
<td>&gt;20 years @ 125°C</td>
<td>0.73mm²</td>
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<tr>
<td>H35, high- temp</td>
<td>1Kx8 bit</td>
<td>EEPROM</td>
<td>2.7 – 3.6 V</td>
<td>2.7 – 3.6 V</td>
<td>40k @ 150°C</td>
<td>10 years @ 150°C</td>
<td>0.94mm²</td>
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<tr>
<td>H35, high- temp</td>
<td>2Kx8 bit</td>
<td>EEPROM</td>
<td>1.8 – 3.6V</td>
<td>1.8 – 3.6V</td>
<td>40k @ 150°C</td>
<td>10 years @ 150°C</td>
<td>1.20mm²</td>
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<tr>
<td>H35</td>
<td>4Kx16 bit</td>
<td>EEPROM</td>
<td>2.7 – 3.6 V</td>
<td>2.7 – 3.6 V</td>
<td>80k @ 125°C</td>
<td>&gt;20 years @ 125°C</td>
<td>1.55mm²</td>
</tr>
</tbody>
</table>

- **Black box delivery: abstract and a Verilog simulation model of the memory**
- **Mandatory 3 days design review with specialized AMS design engineers**
0.18µ CMOS and HV-CMOS
- CMOS technology with ≤ 3 mask level adders for HV
- Three gate oxides available: 1.8, 5V and 20V
- 4 to 7 metal levels (last metal: 4 µm Al power metal)
- Full set of 20 V and 50 V LDMOS devices
- Low Rdson
  - < 14 mΩ*mm²@30 V BVDSS
  - < 130 mΩ*mm²@70 V BVDSS
- 1.8 V and 5 V floating logic (N/PFET)
- High-voltage vertical NPN & PNP bipolar transistors
- Isolated JFET
- High-voltage VN capacitors (20-50V)
- High voltage well based resistors
- 1 kV, 2 kV and 4 kV HBM ESD protection structures
- OTP (Efuse)
- Tool for safe operating area check (SOAC)
Suite of FETs with three gate oxide thicknesses

- Low Voltage (LV) fets for standard 1.8 and 5V CMOS
- LV fets in HV well for high voltage isolation to substrate
- HV asymmetric fets for High Voltage applications
- 3 gate oxide thicknesses, 2 maximum drain bias choices
- HV symmetric fets for specialty applications (transmission gate)

<table>
<thead>
<tr>
<th>Vgs</th>
<th>LV fets</th>
<th>LV fets in HV well</th>
<th>HV asymmetric fets in HV wells</th>
<th>HV symmetric fets (nfet in Substrate)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Vds</td>
<td>1.8V</td>
<td>5.0V</td>
<td>1.8V</td>
</tr>
<tr>
<td>1.8V (3.5nm)</td>
<td>nfet* pfet* nfethvt nfethvt</td>
<td>nfeti* pfeti* nfetihvt nfetihvt</td>
<td>nfeti20t pfeti20t</td>
<td>nfeti50t pfeti50t</td>
</tr>
<tr>
<td>5.0V (12nm)</td>
<td>nfetm pfetm</td>
<td>nfetm pfetm</td>
<td>nfeti20mh nfeti25m pfeti25m</td>
<td>nfeti50m pfeti50m</td>
</tr>
<tr>
<td>20V (52nm)</td>
<td></td>
<td></td>
<td></td>
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</table>

* RF layout available  ** 25V Vds for nfeti25m, pfeti25m
### H18 Passives Key Facts

<table>
<thead>
<tr>
<th>Resistors</th>
<th>Capacitors</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Resistors</strong></td>
<td><strong>Capacitors</strong></td>
</tr>
<tr>
<td>N+ diffusion resistor</td>
<td>Single MIM capacitor</td>
</tr>
<tr>
<td></td>
<td>2.05 fF / µm²</td>
</tr>
<tr>
<td>P+ diffusion resistor</td>
<td>Single MIM HD capacitor</td>
</tr>
<tr>
<td></td>
<td>2.7 fF / µm²</td>
</tr>
<tr>
<td>TaN resistor</td>
<td>Dual MIM capacitor</td>
</tr>
<tr>
<td></td>
<td>4.1 fF / µm²</td>
</tr>
<tr>
<td>N+ poly resistor</td>
<td>Dual MIM HD capacitor</td>
</tr>
<tr>
<td></td>
<td>5.4 fF / µm²</td>
</tr>
<tr>
<td>P+ poly resistor</td>
<td>HiK MIM capacitor</td>
</tr>
<tr>
<td></td>
<td>4.1 fF / µm²</td>
</tr>
<tr>
<td>hires poly resistor</td>
<td>VN capacitor</td>
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<td>0.1-0.7 fF / µm²</td>
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<tr>
<td>Precision poly resistor</td>
<td>HV VN capacitor</td>
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<tr>
<td></td>
<td>0.1-0.5 fF / µm²</td>
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<tr>
<td>TaN resistor</td>
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<tr>
<td>HV Nwell resistor</td>
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<tr>
<td>HV Pwell resistor</td>
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# H18 – 0.18µm High Voltage CMOS

## Technology Availability Status

- Process qualified (jointly with IBM)
- First silicon based HIT-Kit in June 2008, final HIT-Kit since Q4/2010
- Full production since Q1/2011

## Top Benefits

- High performance HV CMOS matching BCD performance
- Several voltage regimes on one chip enables optimized area

## Target Applications

- Power management applications
- MEMS and Sensor interfaces
- Other SOC applications in Medical, Automotive and Industrial

## Process Details

- 1.8V / 5.0V / 20V / 50V
- Gate Density: 118 kGates per mm²
- Low power & low leakage digital libraries
CMOS and HV-CMOS 0.18 μ

- Design-kits available for Cadence.
- C18: 4 MPW runs scheduled in 2014.
- H18: 4 MPW runs scheduled in 2014.
- MPW Price: 1200 Euro/mm² (minimum price 5 mm²)
Activity in 2013
Number of prototypes in 2013: 104 (103 in 2012)
Number of Low volume prod. in 2013: 46 (34 in 2012)

30 scheduled MPW runs (35 in 2012)
7 extra runs (Production) (7 in 2012)

72 circuits CMOS (73 in 2012)
69% (71% in 2012)

20 circuits SiGe (17 in 2012)
19.5% (16.5% in 2012)

12 circuits HV-CMOS (13 in 2012)
11.5% (12.5% in 2012)
AMS Runs Histogram

CMP annual users meeting, 23 January 2014, PARIS
• Low volume productions available in MPW runs. (few hundred to thousand)
• Organized on engineering runs, or production runs.

Low Volume Production runs:

- **IPHIC - Strasbourg / LBNL**: 100 wafers 8" (0.35um CMOS) (Prod. wafers)
- **CEA-Saclay**: 9 wafers 8" (0.35um CMOS)
- **CEA-Saclay**: 18 wafers 8" (0.35um CMOS)
- **NIPSON**: 12 wafers 8" (0.8um BiCMOS) (210,000 circuits)
- **LETI-CEA Grenoble**: 6 wafers 8" (0.35um CMOS)
- **LETI-CEA Grenoble**: 6 wafers 8" (0.35um CMOS)
- **LETI-CEA Grenoble**: 25 wafers 8" (0.35um CMOS) (Prod. wafers)
IPHHC / LBNL / STAR Experiment
Cross-sections: Width = 15µm, depth = 200µm

(Courtesy AMS)

Trench 30mm from edge: 90° / 253µm

(Courtesy AMS)
DRIE trench dicing at AMS, cont’d

(Courtesy AMS)
DRIE trench dicing and thinning ULTIMATE-2 sensors.

- **Project**: ULTIMATE-2 (IPHC / LBNL / STAR Experiment)
- **HRES Epi wafers >400 Ω.cm / DRIE trenching / 50um Wafer thickness**
- **Production of 100 wafers.**
- **Chip dimension**: 20mm x 23mm

DRIE trench dicing and thinning ULTIMATE-2 sensors. The out of plane tolerance is around ~1mm. (Courtesy Lawrence Berkeley National Laboratory for STAR Experiment)
PXL production sensor

- Standard commercial CMOS technology – MAPS
- 3rd generation sensor developed by IPHC for the PXL detector

- Reticle size (~ 4 cm²)
  - Pixel pitch 20.7 μm
  - 928 x 960 array ~890 k pixels
- Power dissipation ~170 mW/cm² @ 3.3V
- Integration time 185.6 μs
- Discriminators at the end of each column
- 2 LVDS data outputs @ 160 MHz
- Zero suppression and run length encoding on rows with up to 9 hits/row
- Ping-pong memory for frame readout (~1500 hits deep)
- 4 sub-arrays to help with process variation
- JTAG configuration of many internal parameters
- Individual discriminator disable, etc.
- Built in automated testing routines for sensor testing and characterization
- High Res Si option – significantly increases S/N and radiation tolerance

10 chips per ladder assembled on FR-4 Handler.

Chip Sensors Designed by IPHC-IN2P3
Integrated by LBNL
Nipson Technology
World record on printing speed (up to 104 meters per minute at 600 DPI resolution)

NIPSON GOING FORWARD
Welcome to NIPSON, a leading provider of digital black and white printing solutions for professional applications. Discover, through our products and solutions, how you can benefit from making these solutions yours.
Low Volume Productions in 2013 increasing in number and quantity.

First Prototypes in 0.18u for CEA-Saclay and IMS-Bordeaux

New processes:
- 0.18µ CMOS & HV-CMOS
- HRES Epi wafers (>400 Ω.cm) 15µ Epi thickness
- DRIE trench dicing

Continuing the strong partnership and collaboration CMP / AMS