UTBB FD-SOI: The Technology for Extreme Power Efficient SOCs

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Technology R&D

Central CAD & Design Solutions
Bulk transistor is reaching its limits

Limited body bias capability

Complex channel architecture

Heavily Doped Wells

Fully Depleted devices are mandatory to continue the technology roadmap

FD-SOI = 2D

FinFET = 3D
### FD-SOI Benefits vs. Other Technologies

<table>
<thead>
<tr>
<th></th>
<th>Bulk</th>
<th>FD-SOI</th>
<th>FD-SOI</th>
<th>FinFET</th>
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<tr>
<td></td>
<td>28 LP</td>
<td>28 G mobile</td>
<td>28FD</td>
<td>14FD</td>
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<td><strong>Power Efficiency</strong> in high performance mode</td>
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<td><strong>Power Efficiency</strong> in low power mode</td>
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<td><strong>Extended DVFS</strong></td>
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<td><strong>ULV capability</strong></td>
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<tr>
<td><strong>Cost</strong></td>
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<td><strong>Process Simplicity</strong></td>
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<td><strong>SER immunity</strong></td>
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<td><strong>Heat dissipation</strong></td>
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<td><strong>Analog Performance</strong></td>
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**Conclusion:**

- 28FD consistently better than any 28nm alternative
- 20nm irrelevant for many segments: better use 28FD or go to 14FD
- 14FD consistently better than 14/FF
28nm Planar UTBB FD-SOI Transistor

Ultra Thin Body & BOX Fully Depleted SOI transistor

36 Masks:
7ML
Dual Vt - Dual Oxide

Thin BOX (25nm)

Substrate

High-K Metal Gate

Thin Body (7nm)
28nm Planar UTBB FD-SOI Advantages

- Shorter channel length
  - 24nm technology!
- Better electrostatics
  - Faster operation
  - Low voltage
  - Reduced variability
- Total dielectric isolation
  - Latch up immunity
- Lower leakage current
  - Less sensitive to temperature

Body-Bias

Hybrid zone

24nm
Cost/Performances Ratios
The FD-SOI Advantage

28nm FD-SOI is same cost as 28LP, same performances as “G” technologies

FD-SOI, the only technology allowing the continuation of the Moore’s law

Source: ST/Marketing 2013, IBS 2013
FD-SOI: the best solution to 10nm

<table>
<thead>
<tr>
<th>Year</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
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</thead>
<tbody>
<tr>
<td>28nm FD-SOI</td>
<td>AVAILABLE TODAY!</td>
<td>MP</td>
<td>MP</td>
<td>MP</td>
<td>MP</td>
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<tr>
<td>14nm FD-SOI</td>
<td>TODAY IN DEVELOPMENT</td>
<td>MP</td>
<td>MP</td>
<td>MP</td>
<td>MP</td>
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<td>10nm FD-SOI</td>
<td>TODAY IN R&amp;D</td>
<td>MP</td>
<td>MP</td>
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<td>MP</td>
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</tbody>
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Advantages of FD-SOI:

- **28nm FD-SOI**:
  - 0.9V
  - 113CPP
  - 90Mx
  - +30% speed
  - -30% power (at same speed)

- **14nm FD-SOI**:  
  - 0.8V
  - 90CPP
  - 64Mx
  - +20% speed
  - -25% power (at same speed)

- **10nm FD-SOI**:  
  - 0.7V
  - 64CPP
  - 48Mx

CPP: Contact to Poly Pitch
Mx: Pitch at Metal layer
A WORLDWIDE DEVELOPMENT ECOSYSTEM

CMOS Technology Alliances
ISDA: 32/28/20 Bulk LP
Pre-T0: 14nm & FDSOI

ST experience enabling the ENERGY EFFICIENCY RACE

2013
2011
2009
2007
2005

90 nm
65/55nm
45/40nm
28nm FDSOI
32/28nm
UTBB FD-SOI Design EcoSystem

- FD-SOI uses a conventional bulk design flow
  - Cadence, Mentor, Synopsys,
  - Apache, Atrenta

- 4-terminals spice models available, from PSP
  - Major simulators supported

- UTBB FD-SOI uses same low power design techniques than for bulk. In addition:
  - Optimized power switches
  - Extended poly-bias
  - Reverse & forward Dynamic body bias
How to migrate Libraries on UTBB

- Full DP re-characterization with dedicated SOI models
  - Charac for various BB conditions depending on the performances targeted
Body Biasing (BB)

A very reasonable effort for extremely worthwhile benefits

- An **extremely powerful** and flexible concept in FD-SOI to:
  - Boost performance
  - Optimize passive and dynamic power consumption
  - Cancel out process variations and extract optimal behavior from all parts

- Comparatively **easy to implement** – if you’ve ever done DVFS you’ll have no difficulty with Body Biasing
  - No area penalty compared to Bulk
  - Reuse of Bulk design techniques
  - Speed/Power control

Back-gate contact
Extended Body Bias Range in UTBB FD-SOI

**Efficient knob for speed/leakage optimization**
Body Bias Efficiency - Silicon Benchmark

- Frequency (MHz):
  - no BB
  - FBB 1V
  - FBB 2V
  - FBB 3V

- Leakage (pA):
  - no BB
  - RBB -1V
  - RBB -2V
  - RBB -3V

- Color codes:
  - 0.5V
  - 1V
  - 1.3V

- FBB
- RBB
### FBB usage per market segment

**Infrastructure - Networking**
- Supply: 0.7 – 0.9V
- High number multicore
- DVFS & FBB tuning for best MIPS/W ratio.
- Adapt perf&power to workload

**Consumer**
- Supply: 0.6 – 1.1V
- Wide DVFS
- FBB linked to CPU workload & thermal conditions

**Internet of Things**
- Supply: 0.6V-0.9V
- Ultra Low Voltage 0.3V-0.4V
- FBB: 0 - 1.5V
- FBB linked to CPU workload & thermal conditions

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Power efficiency</th>
<th>Flexibility Perf/Power</th>
<th>Ultra power efficiency</th>
</tr>
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<tbody>
<tr>
<td><strong>28 FD-SOI:</strong></td>
<td>Up to -50% total power reduction versus 28G(mobile) @ 0.6V</td>
<td>Up to -50% power reduction</td>
<td>Up to x 4 perf/power ratio versus 28G(mobile) at low voltage</td>
</tr>
<tr>
<td>FBB for ultimate power efficiency tuning</td>
<td>FBB provides +18% max. performance boost versus 28G(mobile)</td>
<td>Low voltage power efficient performance. Reduce idle current</td>
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</tr>
</tbody>
</table>
Memories PPA – 28nm FD-SOI vs. 28LP Bulk

For similar Power and Area, large gain in Performance

Data for 4096x32m8 instance
Improved Memory Minimum Voltage

Vddmin on 0.120µm² bitcell

Vddmin -100mV

Mismatch -40% on FDSOI vs. LP

Vmin gain thanks to better mismatch on FD-SOI devices (undoped channel)
ULV Gains Confirmed in 28 FD-SOI Decoder Porting in 28 FD-SOI

• Intrinsic FD-SOI advantage for ULV
  • Electrostatic control enhancement → speed at low voltage
  • Undoped homogeneous channel → Reduced variability
  → Lower minimum usable supply voltage

Real silicon measurement on ULV DSP
BULK vs FDSOI Yield
FD-SOI enabling Ultra-Wide DVFS

- FD-SOI allows the widest Vdd range for voltage scaling
- Still guaranteeing top notch speeds at very low operating voltage
  - >5x when compared to 28LP technology
  - >35% when compared to 28G technologies

Real measurements of continuous DVFS in the range 0.5V – 1.4V
Performed on a very large number of ICs, showing extremely good reliability of the DVFS in this range
FD-SOI: Analog Technology

**Complex channel architecture**
- Source of variability

**Heavily Doped Wells**
- High variability due to dopant fluctuation
- Low analog gain due to pocket implant

**Total dielectric isolation**
- Lower S/D capacitances
- Lower S/D leakages
- Latch-up immunity

**No channel doping**
- Better matching for short channel devices
- Lower 1/f noise

**No pocket implant**
- Better gain compared to bulk

**New design opportunity** by controlling analog device characteristics through **body biasing** techniques.
Best in Class SER performances with FDSOI

- **SRAM-SER tested** $\times 100$ better with FDSOI28 compared to CMOS 28nm
  - combining both alpha and neutron gains

- **Very low neutron-SER** $<$10 FIT/Mb
  - ECC not systematically required
  - power and area savings

- **Alpha immunity**
  - Ultra Low Alpha not required
  - packaging cost savings

![Diagram showing neutron-SER comparison between different technologies with FDSOI28 having the lowest SER.](image-url)
UTBB FD-SOI:
Half Node Effort for Full Node Benefit

- **CPU**
  - Dual Cortex A9
  - +40% in speed
  - > 3X at low V

- **GPU**
  - SGX544 MP1
  - +20% at nom V
  - Power reduction

- **HD camera IP**
  - +30% in speed

- **PLLs**
  - Up to 4.6GHz
  - -15% in power

- **LPDDR2 533Mhz**
  - -15% in power
28nm FD-SOI Best in class efficiency

@ low Vdd
+43% vs 28LP
+83% vs 28G

@ high Vdd
+50% vs 28LP
+25% vs 28G

Energy efficiency (relative DMIPS/mW)

Speed (relative DMIPS)

@ low Vdd
@ high Vdd (overdrive)
FD-SOI
The best technology choice

Superior and flexible technology

• FD-SOI transistors are faster, cooler, simpler
• Outstanding power efficiency across all use cases
• Efficiency at all levels: CPU, logic, Memories, Analog
• Manufacturing infrastructure and process reuse
• Improved reliability

Enhanced design options

• Very large operating range for the same design
• Back-biasing as a flexible and powerful optimization
• Ultra-wide range DVFS
• Enhanced efficiency of multi-core processing
• Easier design than FinFET

Gives your SOC competitive advantages

• Costs: chip-level and/or system-level (e.g. cost of cooling)
• Thermal power dissipation (TDP)
• Extended battery life
• Computing Power / Speed / Reactivity
• Reliability
• Time-to-Market