Packaging Services

MPW Services Center for IC / MEMS Prototyping

http://cmp.imag.fr

Grenoble - France
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• **Regular Packaging process flow**
  • Shipment for and Dicing (about 2 weeks)
  • Shipment an packaging (nominal 2-3 weeks and up to weeks for special requests and with foreign subcontractors)
• **Back grinding**

8” wafers (200 mm): 725 µm (+/- 20µm) standard thickness
12” wafers (300 mm): 780 µm (+/- 20µm) standard thickness

**Wafer level back grinding**

- ams:
  - 0.35 µm (8”) => standard back lapping to 530 µm
  - => back lapping to 250 µm on request

- STMicroelectronics:
  - 130 nm (8”) => standard back lapping to 375 µm
  - 65 nm (12”) => standard back lapping to 250 µm
  - 28 nm (12”) => standard back lapping to 250 µm

**Die level back lapping**

- Down to 150 µm (absolute limit 100 µm)
- Minimum 10µm roughness on backside!
• Bonding technics

Thermo-Sonic Method: Ball-Bonding

- Pure and hardened Gold wires
- Diameter wires from 15 µm up to 80 µm
- Few packaging constraints

Ultra-Sonic Method: Wedge-Bonding

- Aluminum wires from 25µm up to 500 µm
- Allow high voltage and power applications
- Interconnection density smaller
Package selection guidelines

Ceramic or Plastic?

• Prototyping:
  CMP recommends to use ceramic packaging
  Advantages:
   - Price for small quantities
   - Removable lids
   - Flexible constraint (wire length, ground bonds, die thickness
   - Thermal, high-reliability (Space qualification)

• Low volume:
  CMP recommends to choose the plastic package
  Advantages:
   - Low cost from 20-40 packaging (open tool only)
   - Access to density solutions for “low price” (PBGA)
  Longer process time!
• Available packages

Sealed or Removable Lids

- Dual In-Line
- Pin Grid Array
- CerQuad Flat Pack.
- Leadless & J-Leaded Chip Carrier
- Small Outline
- Quad Flat No lead
- Thin Quad Flat Package
• How to make a good bonding diagram!

  • A: Chose a package with the right number of pad by side
  • B: Connect pads to pins in front of Them
  • C: Use a regular spacing between pads
  • D: Have a regular space between wires
• How to make a good bonding diagram!

• E: Use all the length for your pads

• F: Use the shortest wire

• G: You should have the same number of pad and pins on the same side of the package

• H: Bonding pads have to be perfectly aligned near circuit edges
Available packages
- Leaded

QFP Family
- Plastic Leaded Chip Carrier
- Metric Quad Flat Package
- Thin Quad Flat Package
- Low Quad Flat Package
- Small Outline

Thin, array, leadless
- Thin Shrink Small Outline Package
- Plastic Ball Grid Array
- Fine pitch Ball Grid Array
- Quad Flat No lead
• **Bonding diagram rules**
  - Double Pad ring have to be checked by CMP engineers
  - Wire length have to be less than 3mm long
    - To avoid short circuits during the final packaging step
    - Connections to center pad have to be checked by CMP

• **Special turnaround**
  - During a MPW run: minimum 3 weeks, more than ceramic assemblies
  - Additional packaging: depend on the availability of the packages when packaging is performed
• Not reliable
  
  • Center pads connected
  
  • Wires in corners too close
Advantages:
- Open cavity packages enable smooth transfer to plastic packaging process
- Price for small quantities up to 20-40 dies
- Open cavity process is universal and can be applied to any plastic IC package: BGA, QFP, QFN, PLCC, SOIC, TSSOP and more…
Interposer MPW services
• **New offer in partnership with ams and CEA-LETI**
  
  • First run: 16\(^{th}\) November 2015
  
  • Price/mm\(^2\): check on our web site or contact us
  
  • Turnaround: 16 weeks

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• **New Packaging possibility**
  
  • Flip chip assemblies on silicon interposer
  
  • High density interconnections between two or more different and heterogeneous designs
  
  • Interposer wire bonded to PCB or package!
• Based on ams 0.35um Metal stack (3+1Th) + UBM

• Design kit
  • Standard CMOS 0.35um ams design kit + UBM DRM
  • Specific interposer design kit will be available soon for customers who don’t have access to the standard design kit
Open 3D advanced packaging MPW services
• **New offer in partnership with CEA-LETI**
  • Post processes offered after STMicroelectronics/ams MPW runs

• **Lower the cost of silicon for 3D prototyping and share the costs of post processing**
  • Available on standard MPW run
  • Sharing the packaging cost
  • CMP owns the wafers, and guarantees all project confidentiality. All parts are given back to CMP for inspection after post processing. MPW confidentiality guaranteed.

• **1 run/process/year available**
• Operated as a post processing toolbox:
  • Three packaging options

- Die-to-substrate
- Die-to-interposer
  Or Die to Die
- Flip Chip stacking + TSV Last stacking
• **BUMPS (for 0.35µm ams, 130 and 65nmST processes)**
  - Pad size: 55 um => allowed customer to have some sample in package for standard test
  - Pitch: 120 um
  - Bumps size: 65 um

• **MicroBUMPS (for 28nmST)**
  - Pad size: 40 um
  - Pitch: 50 um
  - Bumps size: 25
• **TSV (available on 130 and 65nm ST processes)**
  - TSV size: 60 μm
  - Pitch: 120 μm
  - RDL material: Cu / protective layer possible
  - RDL thickness: 1-10 μm
  - RDL minimum width: 20 μm
  - RDL minimum space: 20 μm

• **UBM**
  - UBM material: TiNiAu
  - UBM thickness: 0.5 – 1.5 μm
  - UBM width: 20 – 800 μm
  - UBM minimum pitch: 40 μm
• Compatibility with substrate or interposer packaging
  • CMP can manage flip chip on substrate or silicon interposer
    • Substrate can be furnished (but assembly is not guaranteed)
    • Substrates can be supplied thanks to specifications
      • Substrates can be organic or ceramic

Die-to-interposer
• **ams turnaround**

  - DRC: 2 weeks
  - Fab Start: 6 weeks
  - 3D post process: 12 weeks
  - Dicing: 3 weeks
  - Packaging: 3 weeks minimum
  - **Total: 26 weeks**

• **ST 65nm turnaround**

  - DRC: 3 weeks
  - Fab Start: 13 weeks
  - 3D post process: 12 weeks
  - Dicing: 2 weeks
  - Packaging: 3 weeks minimum
  - Bumped Dies: 3 weeks minimum
  - Bumped Dies: 3 weeks
  - Packaged dies: 3 weeks minimum
  - **Total: 34 weeks**
- **Pricing method:**
  - A fixed fee + a fee depending on chip size
  - Assembly on substrate not included

<table>
<thead>
<tr>
<th>Technologies</th>
<th>IC surface (mm²)</th>
<th>Fixed fee (k€)</th>
<th>/mm² (k€)</th>
<th>Additional fees (k€)</th>
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Guaranteed minimum delivered pieces 40 without extra charge

Applicable only in 0,35μm ams and 130, 65 and 28nm ST for projects and wafers processed through CMP, otherwise, please contact us

(1) Includes, additional passivation, seed layer, copper pillar and soldering capping
(2) Additional fees: 3k€ in 130nm / 7k€ in 65nm / 11k€ in 28nm ST processes, 4k € ams process other request, please contact us
(3) Flip chip made by CMP on provided substrate: 5k€
## Open 3D Prices (2/2)

<table>
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<th>Technology</th>
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<th>Additional fees (k€)</th>
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 Guaranteed minimum delivered pieces 40 up without extra charge
 Applicable only in 130nm and 65nm MPW for projects and wafers processed through CMP, otherwise, please contact us
 (1) Requires to use appropriate PDK, Includes grinding, TSV, RDL and Under Bump Metallization on both sides of the IC
 (2) Additional fees 4k€ in 130nm / 10k€ in 65nm
 (3) Option with back side bump deposition : on request
 (4) Option for assembly on provided substrates: 5k€ for 40 pieces
 UBΜ² means UBΜ made on both sides of the chip.
- **Design kit provided by CMP**
- **Compatible processes**
  - 0.35µm ams (bumps only)
  - 130 nm CMOS
  - 130 nm BiCMOS
  - 65 nm CMOS
  - 28 nm FDSOI (micro bumps only)
- **Schedule**
  - First one: October /November MPW
  - Turnaround: 6 months
- **3D packaging**
  - CMP can manage assembly to substrate
  - CMP can provide organic/ceramic substrate

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Thank you!