Design-Kits, Libraries and IPs

MPW Services Center for IC / MEMS Prototyping

http://cmp.imag.fr

Grenoble - France
AMS Design-Kits
- Supported CAD tools
- Libraries provided
- IPs available

ST Design-Kits
- Supported CAD tools
- Libraries provided
- IPs available

MEMS Design-Kits
Technology names

- 0.35μm CMOS
  - 0.35μm CMOS-Opto
  - 0.35μm CMOS RF

- 0.35μm HV-CMOS → C35

- 0.35μm SiGe → S35

- 0.18μm CMOS → C18

- 0.18μm HV-CMOS → H18
### Current distributions:

<table>
<thead>
<tr>
<th></th>
<th>Cadence (SUN / Linux)</th>
<th>Mentor (SUN / Linux)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CDB</td>
<td>OA</td>
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<tr>
<td>C35 (0.35µm CMOS)</td>
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<td>S35 (0.35µm SiGe)</td>
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<tr>
<td>C18 (0.18µm CMOS)</td>
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<td>H18 (0.18µm HV-CMOS)</td>
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## Supported CAD tools:

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<thead>
<tr>
<th></th>
<th>Schematic &amp; Design Entry</th>
<th>Electrical Simulation</th>
<th>Digital Simulation</th>
<th>Logic Synthesis</th>
<th>Layout &amp; Verification</th>
<th>P&amp;R</th>
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<tbody>
<tr>
<td><strong>Cadence</strong></td>
<td>Cadence</td>
<td>Spectre</td>
<td>NC-Sim</td>
<td>RTL Compiler</td>
<td>Virtuoso</td>
<td>Encounter Digital</td>
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<td></td>
<td>Composer</td>
<td>Hspice</td>
<td>AMS-Designer</td>
<td></td>
<td>Assura</td>
<td>Implementation (EDI)</td>
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<td>Ultrasim</td>
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<td>QuestaSim</td>
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<td>Hspice</td>
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<td><strong>Tanner</strong></td>
<td>Tanner S-Edit</td>
<td>TSpice</td>
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<td>L-Edit</td>
<td>SPR</td>
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</table>
• If you are facing issues on the design kits installation or during the tools usage, please send an email to

cmp-support@imag.fr
AMS Libraries

- LV Digital standard cells and IO Libraries:
  - CORELIB and CORELIB_3B: General purpose digital library
  - IOLIB: IO pads (input, output, bidir.) 3.3V and 5V available
  - IOLIBC_3B: Core limited digital IO Libraries

- HV Digital standard cells and IO Libraries:
  - CORELIB_HV: CORELIB for high voltage.
  - IOLIB_HV: High Voltage digital IO pads library

- Analog standard cells Libraries:
  - IOLIB_ANA: Analog IO pads library
  - IOLIBC_ANA_3B: Core limited Analog IO pads library
  - IOLIB_ANA_HV: High Voltage Analog IO pads library
  - A CELLS: Analog Library

- RF standard IO cells Libraries:
  - SPIRAL: Library with characterized inductors
  - RF_PADS: RF IO pads library
Some IP blocks are available and free of charge to Univ. & Research (0.35µ CMOS):

<table>
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<tr>
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<td>4098</td>
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</table>

Single & Dual Port RAMS Configurations
Agenda

- AMS Design-Kits
  - Supported CAD tools
  - Libraries provided
  - IPs available

- ST Design-Kits
  - Supported CAD tools
  - Libraries provided
  - IPs available

- MEMS Design-Kits
Technology names

- 16µm Bipolar – CMOS – DMOS → BCD8SP
- 130nm
  - 130nm CMOS → HCMOS9GP
  - 130nm HV-CMOS → HCMOS9A
  - 130nm SiGe → BiCMOS9MW
  - 130nm SOI → H9SOI-FEM
- 65nm CMOS → CMOS065
- 55nm CMOS → BiCMOS55
- 28nm FD-SOI → CMOS28FD-SOI
### Current distributions

<table>
<thead>
<tr>
<th>Design Kit</th>
<th>Version</th>
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<tbody>
<tr>
<td>BCD8SP</td>
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<td>CMOS28FDSOI</td>
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RF option is available for HCMOS9GP and CMOS065 design kits.
## Supported CAD tools:

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<th>Verification</th>
<th>Parasitic extraction</th>
<th>P&amp;R</th>
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<td>ICC (SNPS)</td>
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| HCMOS9GP            | X         | -          | X X X X               | -    |
|                     |           | -          | -                     | X    |
|                     |           |            | X X                   | -    |
|                     |           |            | X                     | X    |
|                     |           |            | X                     | X    |
|                     |           |            | X                     | X    |
| BiCMOS9-MW          | X X       | X X X X    | X X                   | X X  |
|                     |           |            | X X                   | X X  |
| HCMOS9A             | X X       | X X X X    | -                     | -    |
|                     |           |            | -                     | X    |
|                     |           |            | X                     | -    |
|                     |           |            | X                     | X    |
| H9SOI-FEM           | - X       | X X X X    | -                     | X X  |
|                     |           |            | X                     | -    |
|                     |           |            | X                     | X    |
| CMOS065             | X X       | X X X X    | X X                   | X X  |
|                     |           |            | X                     | X    |
|                     |           |            | X                     | -    |
|                     |           |            | X                     | X    |
| BiCMOS55            | - X       | X X X X    | X X                   | X X  |
|                     |           |            | X                     | -    |
|                     |           |            | X                     | -    |
| CMOS28FDSOI         | - X       | X X X X    | X                     | X X  |
|                     |           |            | X                     | X    |
|                     |           |            | X                     | X    |

**Supported CAD tools:**

- **HCMOS9GP**: X - X X X X - - X - X - - X X
- **BiCMOS9-MW**: X X X X X X X X X - X X X
- **HCMOS9A**: X X X X - - - X - X - - - X
- **H9SOI-FEM**: - X X X X - X X X - X X - -
- **CMOS065**: X X X X X X X X - X X - X X
- **BiCMOS55**: - X X X X X X X X - X - - -
- **CMOS28FDSOI**: - X X X X X - X X X - X X X
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cmp-support@imag.fr
• **CORE cells Libraries:**
  - **CORE**: General purpose core libraries
  - **CORX**: Complementary core libraries (complex gates)
  - **CLOCK**: Buffer cells and the same for clock tree synthesis
  - **PR**: Place and route filler cells and the same.
  - **DP**: Datapath leaf cells libraries
  - **HD**: High density core libraries

• **IO cells Libraries:**
  - 1.8V, 2.5V, 3.3V IO pads:
    - 80µ, 65µ, 60µ, 50µ 40µ and 30µ IO pads: Digital and Analog
    - Staggered IO pads
    - Flip-Chip pads
    - Level Shifters, and compensation cells
Generation of RAM/ROM is free of charge for fabrication of circuits.
Lead-time for memory generation is 1 to 2 weeks.

**Types of generators:**

- **SPREG:** single port register
- **SPRAM:** single port RAM
- **DPREG:** dual port register
- **DPRAM:** dual port RAM
- **ROM**

<table>
<thead>
<tr>
<th>Technology</th>
<th>SPREG</th>
<th>SPRAM</th>
<th>DPREG</th>
<th>DPRAM</th>
<th>ROM</th>
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<td>CMOS28FDSOI</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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</table>
**Cut Explorer** at STMicroelectronics allows selecting the best configuration of RAM/ROM. The tool is configured for all technologies except for CMOS28FDSOI.

**Inputs:**
- Type of block: SPRAM, DPRAM, ROM
- Size: number of words, number of bits per word

**Outputs:**
- Cut name: all parameters for block generation are coded in cut name
- Sizing information: X, Y, area, number of MUX, ...
- Timing information
- Power information

**RAM/ROM generators:**
Flow for a request of block (1 or 2 weeks):

- Send to CMP type, number of words and number of bits
- Receive results of Cut explorer
- Send names of selected cuts
- Generation at STMicroelectronics, data preparation at CMP (reduced layouts)
- Delivery of blocks. Data include layout, models for simulation, files for P&R.
Agenda

AMS Design-Kits
- Supported CAD tools
- Libraries provided
- IPs available

ST Design-Kits
- Supported CAD tools
- Libraries provided
- IPs available

MEMS Design-Kits
### MEMS Design-Kits

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Technology</th>
<th>Design kit</th>
<th>Software</th>
<th>Version</th>
<th>Fields of application</th>
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<td>amvis</td>
<td>Bulk Micromachining</td>
<td>HIT-Kit_ams_4.10</td>
<td><a href="#">Cadence</a></td>
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<td>Physical layout and DRC</td>
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<td><a href="#">Tanner EDA</a></td>
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<tr>
<td>TELEDYNE BALSA</td>
<td>MIDIS</td>
<td>MK15S1</td>
<td><a href="#">COVENTOR</a></td>
<td>Catapult (Designer) from CoventorWareTM</td>
<td>Physical layout, design entry and multi-physics analysis</td>
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<td><a href="#">Virtuoso Layout Suite</a> ver.1C6.1.5 from Cadence</td>
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<td><a href="#">L-Edit</a></td>
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Thank you!