STMicroelectronics
Deep Sub-Micron Processes
0.18µ, 0.12µ, 90nm CMOS
• Higher the density
• Lower the power
• More system Integration
• More Process Features

1994 at CMP

AMS 0.8µ
1.2k gates/mm²

AMS 0.6µ
3k gates/mm²

AMS 0.35µ
18k gates/mm²

ST 0.25µ
35k gates/mm²

ST 0.18µ
80k gates/mm²

ST 0.12µ
180k gates/mm²

ST 90nm
400k gates/mm²

2004 at CMP
Feature size, 1983 - 2010

- **Industry (SIA where available)**
- **CMP**

![Graph showing feature size from 1983 to 2010](image-url)
STMicroelectronics CMOS 0.18 μ

HCMOS8D
HCMOS8D Process Features

- 0.18µ mixed A/D CMOS SLP/6LM
- Gate length (0.18 µm drawn, 0.15 µm effective).
- Shallow trench isolation process.
- Up to 6 levels metal layers with fully stackable contacts and vias.
- MIM precision capacitors.
- Power supply: 1.8 V. (Abs. Maximum 1.95 V)
- Threshold voltage: VTN = 0.5 V, VTP = - 0.5 V.
- Ion : TN @ 1.8 V : 500 µA/µm
- Ion : TP @ 1.8 V : 210 µA/µm
**Metal/Metal Capacitors:**

- Metal5/Metal5-bis in HCMOS8D

**2 types of MOSes in HCMOS8D:**

- High Performance MOSes
- Low Leakage MOSes.
HCMOS8D Process

Introduced by CMP in Q4 99
~ 120 centers received design rules and design-kits

• 1 Last MPW run in 2005  (2 runs in 2004)
• 1 circuit fabricated  (15 circuits in 2004)

• MPW stopped in 2005.

![Graph showing mm² area for years 2001 to 2005]
STMicroelectronics CMOS  0.12 µ
HCMOS9
HCMOS9 Process Features

- 0.12µ mixed A/D CMOS SLP/6LM (triple Well)
- Gate length (0.13 µm drawn, 0.11 µm effective).
- 6 Cu metal layers. (Up to 8 metal layers in option)
- Low k inter-level dielectric
- Power supply: 1.2 V
- Multiple Vt transistor offering
  (Ultra low leakage, low leakage, High speed)
- Threshold voltages (for 3 families above):
  VTN = 570/500/380 mV, VTP = 590/480/390 mV
- Isat (for 3 families above):
  TN @ 1.2 V : 410/535/680 uA/mic; TP @ 1.2 V : 170/240/320 uA/mic
0.12µ mixed A/D CMOS SLP/6LM introduced by CMP in Q4 2001

~ 110 centers received design rules, design-kits (80 in 2004)

- 7 runs organized in 2005
- 60 circuits (13 from France + 47 abroad)

- 2500 Euro/mm²
  (25 samples for which 5 are packaged)

- Open to every Institution or Company. (under NDA)

HCMOS9 Process

6 levels Cu Metal (Cross Section View) Courtesy STMicroelectronics

2003 2004 2005

0 50 100 150 200 250 300 350 400

mm²
STMicroelectronics CMOS  90nm

CMOS090
• 65nm poly length (90nm drawn)
• Triple Vt MOS transistors
• Dual gate oxide
• Dedicated process flavors for high performance or low power
• Dual-damascene copper for interconnect.
• 7 metal layers for interconnection
• 0.28um metallization pitch.
• Analog / RF capabilities.
• Fully compatible with e-DRAM
• Various power supplies supported: 3.3V, 2.5V, 1.8V, 1.2V, 1V
• Dual standard cell libraries (speed / density)
  (430 kgates/mm2 / 350 kgates/mm2).
• Total of > 1000 core cells
• Gate delay of 11ps (standard Vt)
• Embedded memories SRAM / ROM
90nm mixed A/D CMOS 7LM introduced by CMP in Q3 2004

100 customers received design rules, design-kits

- 7 MPW runs planned in 2005
- 5000 Euro/mm²
  (25 samples for which 5 are packaged)
- Open to every Institution or Company, (under NDA).
| University of Parma                | ITALY                |
| University Of Modena And Reggio Emilia | ITALY                |
| Tohoku University, Sendai           | JAPAN                |
| Norwegian Univ. of Sc. & Techno., Trondheim | NORWAY            |
| University of Oslo                 | NORWAY                |
| University Of The Philippines, Diliman | PHILIPPINES        |
| St. Petersburg State University    | RUSSIA                |
| Taganrog State Univ. Of Radioengineering | RUSSIA            |
| Moscow Institute Of Electronic Technology | RUSSIA            |
| Nanyang Technical University, Singapore | SINGAPORE        |
| Universidad de Zaragoza            | SPAIN                 |
| Universitat Politecnica De Catalunya | SPAIN               |
| InstitutoMicroelectronica Sevila   | SPAIN                 |
| Chalmers University of Technology  | SWEDEN                |
| Linköping University              | SWEDEN                |
| Mid Sweden University, Sundsvall   | SWEDEN                |
| ETH Zurich                        | SWITZERLAND            |
| Université de Neuchâtel            | SWITZERLAND            |
| CERN, Geneva                      | SWITZERLAND            |
| NECTEC, Bangkok                   | THAILAND              |
| University College London         | UK                    |
| Imperial College of Science, London | UK                  |
| Lime Microsystems &d, Haslemere   | UK                    |
| University of Bath                | UK                    |
| University Of Edinburgh           | UK                    |
| University Of Glasgow             | UK                    |
| University Of Manchester          | UK                    |
| University Of Sheffield           | UK                    |
| Achronix Semiconductor Llc, Ithaca NY | USA                |
| Berkeley Wireless Research Center | USA                  |
| Carnegie Mellon University, Pittsburgh | USA              |
| Columbia University, New York     | USA                  |
| Forza Silicon Corp., Pasadena, CA | USA                  |
| Johns Hopkins University          | USA                  |
| MIT, Cambridge                    | USA                  |
| Stanford University               | USA                  |
| SiBEAM Inc, Fremont               | USA                  |
| Sun Microsystems Inc., Mountain View, CA | USA            |
| UCLA, Los Angeles, Ca            | USA                  |
| University Of Santa Cruz          | USA                  |
| University Of Michigan            | USA                  |
| University of Rochester           | USA                  |
| Washington State University, Pullman | USA               |
| University Of Texas At Dallas     | USA                  |

**CMP annual users meeting, 13 January 2006, PARIS**
32 designs have been fabricated in 90nm CMOS in 2005.

14 customers have submitted their designs:

- Berkeley Wireless Research Centre (BWRC, USA)
- ETH-Zurich (Switzerland)
- Sun Microsystems (USA)
- UCLA (USA)
- University of Stuttgart (Germany)
- VTT (Finland)
- INFN (Italy)
- University of Oslo (Norway)
- Norwegian University of Science and Technology (Norway)
- Stanford University (USA)
- CMC Microsystems (Canada)
- University of Pisa (Italy)
- Massachusetts Institute of Technology (MIT) (USA)
- Achronix Semiconductor LLC (USA)
BiCMOS6G Process From STMicroelectronics

STMicroelectronics SiGe 0.35μ

BICMOS6G
BiCMOS6G process specifications

- Complementary bipolar process with vertical NPN & vertical isolated PNP
- Single layer poly / 5 layers metal
- Metal 5 is thick 2.5 µ Alu (high Q inductances, power supplies)
- MIM capacitors available: 2nF/mm² and 5nF/mm²
- High resistive poly: 1 kΩ/sq
- NPN 3.3 V ($F_T = 45$ GHz, $= 0.8$ dB)
- NPN 5.0 V ($F_T = 25$ GHz)
- Standard Power Supplies: 3.3 V or 5.0 V
BICMOS6G
SiGe HBT transistor architecture

Schematic cross section of SiGe HBT

SEM cross sectional view of SiGe HBT
Vertical Isolated PNP structure
(Poly base emetteur)
Isolated NMOS
Applications

- High performance RF designs
  - HBT components with high $F_t$ and low noise.
  - High Q integrated passive components (R, L, C)
- High Performance mixed A/D designs
  - HBT bipolar + CMOS : Excellent Analog environment
  - Standard digital cells libraries
- System on chip designs
  - High density CMOS digital library
  - N-ISO layer for blocks isolation (RF / Analog / Digital / …)
MPW runs

- Introduced at CMP in 2000
  50 customers received design rules and design-kits

- 950 Euro/mm²
  - Minimum charge is the price of 3 mm².
  - Delivery of 25 samples for which 5 are packaged.
  - Open to every Institution or Company, (under NDA).

- 3 MPW runs scheduled in 2006.
BiCMOS7RF Technology

0.25µm SiGe:C BiCMOS process
For RF and Power Applications

Cellular Terminals Division
BiCMOS Technologies

- **BiCMOS9**
  - 0.13μm CMOS
  - SiGe-C, fT/Fmax=150GHz/150GHz

- **BiCMOS8X**
  - 0.18μm CMOS
  - SiGe, fT/Fmax=70GHz/90GHz

- **BiCMOS7**
  - 0.25μm CMOS
  - SiGe, fT/Fmax=70GHz/90GHz

- **BiCMOS6G**
  - 0.35μm CMOS
  - SiGe, fT/Fmax=45GHz/60GHz

- **BiCMOS6/6M**
  - 0.35μm CMOS
  - Si, fT/Fmax=25GHz/40GHz

- **BiCMOS7RF**
  - 0.25μm CMOS
  - SiGe-C, fT/Fmax=60GHz/90GHz

CMP annual users meeting, 13 January 2006, PARIS
BiCMOS7RF Definition & Objectives

- The next technology for RF applications (after BiCMOS6G)

- An optimization of BiCMOS7 to address RF needs, BiCMOS7 being more dedicated to optical networks market (f >5Ghz).

- Compared to BiCMOS6G, BiCMOS7RF:
  - Have a better HF noise figure
  - Reduced substrate coupling
  - Allow power amplifier integration
  - Offer high performance passive devices
  - Increase CMOS density
• CMOS
  – Use of HCMOS7 as the base process
  – 5 nm gate oxide
  – 0.25 µm gate length
  – Shallow trench isolation
  – Gate type N+ and P+
  – Silicidation of gates and junctions for low access resistance
  – Supply voltage 2.5V (2.7V max)

• 50W.cm SUBSTRATE
General Features 2/3

• **BIPOLAR**
  – **SiGe:C** epitaxial base (non selective)
  – Deep trench isolation
  – Quasi self aligned structure
  – Low-voltage HBT (Ft=55GHz typ – BVCEO=2.8V min)
  – High-voltage HBT (Ft=30GHz typ – BVCEO=6.0V typ)
  – Low Noise Characteristics (Nfmin=0.4dB at 2GHz)

• **OTHER DEVICES**
  – Polysilicon resistors: P & N type (85 & 180W/sq)
  – N+ Active resistor (60W/sq)
  – Poly/N+ sinker capacitor (2.88fF/µm²)
General Features 3/3

• OPTIONS
  – HV NLDEMOS (2.5V – BVDS=13.5V min – WxRon=3W.mm typ)
  – High value poly resistor (1kW/sq)
  – Isolated N-channel MOS
  – Isolated Vertical PNP (Ft=6GHz typ – BVCEO=9.5V typ)
  – 5fF/µm² MIM capacitor
  – Precise TaN resistor (35W/sq; +/-10%)

• BACK END
  – 5 metal levels / thick top metal 2.5µm
  – M1 in Tungsten; M2 – M5 in Aluminium
  – M5 in thick copper 4µm (option)
  – Bumping
# BiCMOS7RF Devices List

## MOSFETs
- 2.5V N&P MOSFETs
- Drift N&P MOS transistors
- Isolated NMOS transistor
- HV NLDEMOS transistor (option)
- LV NLDEMOS transistor (option)
- LV PLDEMOS transistor (option)

## Bipolar Transistors
- Low-voltage SiGe:C NPN HBT
- High-voltage SiGe:C NPN HBT
- Isolated vertical PNP BJT (option)
- Lateral PNP transistor

## Capacitors
- 5fF/μm² MIM capacitor
- N+ Poly/NWell capacitor
- N+ Poly/N+ Sinker capacitor

## Junction Diodes
- N+/Pwell
- P+/Nwell

## Varactors
- P+/Nwell diode
- P+/Nwell diode with differential structure
- MOS transistor

## Resistors
- Silicided N+ Poly
- Unsilicided N+ Active
- Unsilicided N+ Poly
- Unsilicided P+ Poly
- Nwell under STI
- Hipo
- Precise TaN (option)

## Thick Metal Inductors
- Single-ended inductors
- Symmetrical and differential inductors
## Technological Masks

- **Core Process (2.5V CMOS, HBTs)** 29 masks
- **PA Bipolar Cell** free
- **HV NLDEMONS option** 2 masks
- **IVPNP BJT option** 2 masks
- **Isolated NMOS option** 1 mask (free if IVPNP)
- **High Value Poly Resistor (hipo) option** 1 mask
- **5fF/μm² MIM Capacitor option** 1 mask

### Future Option
- **Precise TaN Resistor** 1 mask
- **LV NLDEMONS option** 2 masks (1 if HV NLDEMONS)
- **LV PLDEMONS option** 2 masks
BICMOS7RF MPW runs

- 1500 Euro/mm²
  - Minimum charge is the price of 3 mm².
  - Delivery of 25 samples for which 5 are packaged.
  - Open to every Institution or Company, (under NDA).

- 3 MPW runs expected in 2006.
Common Advices to all ST processes:

- Special care on Minimum and Maximum densities for each layer:
  - Especially for the analog and RF circuits.
  - Design submission: Inform CMP on your requirements for dummies filling.

- Special attention to the MIM capacitor layout design.

- Padrng: should always use the IOFILLER cells for pad abutments.

- Special attention to the type of CORNER cells to use (contact CMP for more information)
MPWs IN 2005

15 MPWs, 1 taxi, 96 circuits, 577 mm²

- HCMOS9GP: 7 MPWs, 60 circuits, 375 mm²
- CMOS090: 6 MPWs, 32 circuits, 165 mm²
- BiCMOS6G: 1 MPW, 2 circuits, 23 mm²
- BiCMOS7RF: 1 MPW, 1 circuit, 10 mm²
- HCMOS8D: 1 taxi, 1 circuit, 4 mm²
EVOLUTION 2004/2005
(number of circuits)
TYPES OF CIRCUITS

Industry: 13, Research: 66, Education: 13

* Data for Europe include France