

3D-IC Integration

- **Developments**
- **Cooperation for servicing and MPW runs offering**

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- **Introduction & Motivation for 3D-IC**
- **Process overview**
- **Partnership for MPW runs service**
- **3D-IC Design Platform**
- **Conclusion**

3D-IC Integration : Not a New Story

Akasaka, Y., and Nishimura, T., "Concept and Basic Technologies for 3-D IC Structure"
 IEEE Proceedings of International Electron Devices Meetings, Vo. 32, **1986**, pp. 488-491.

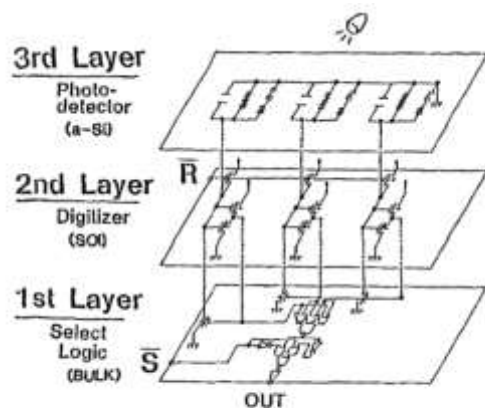


Fig.8 a-Si photo sensor and processing circuits in 3-staked layers (after Mihashi)

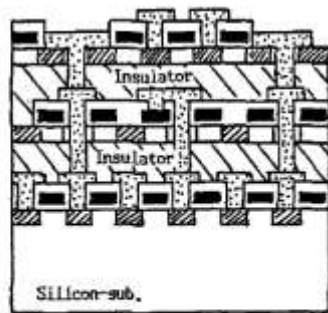


Fig.1 Schematic drawing of 3-D IC consisting of monolithic multi-layer structure.

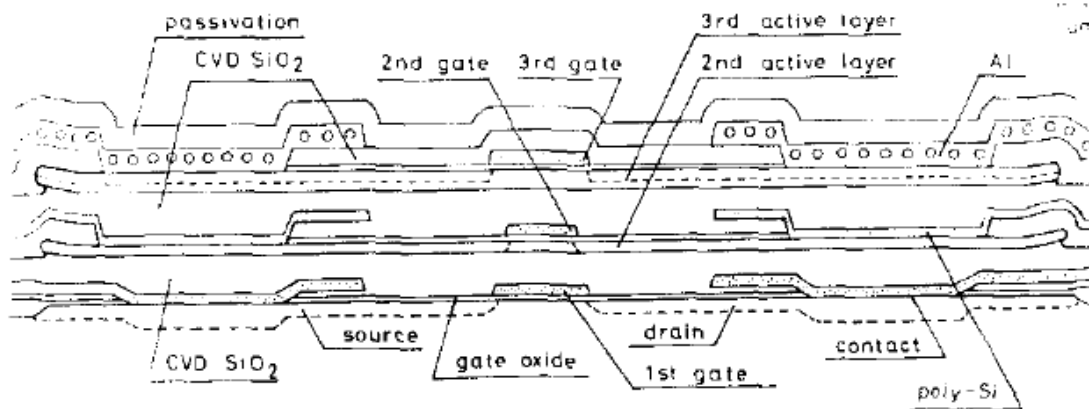
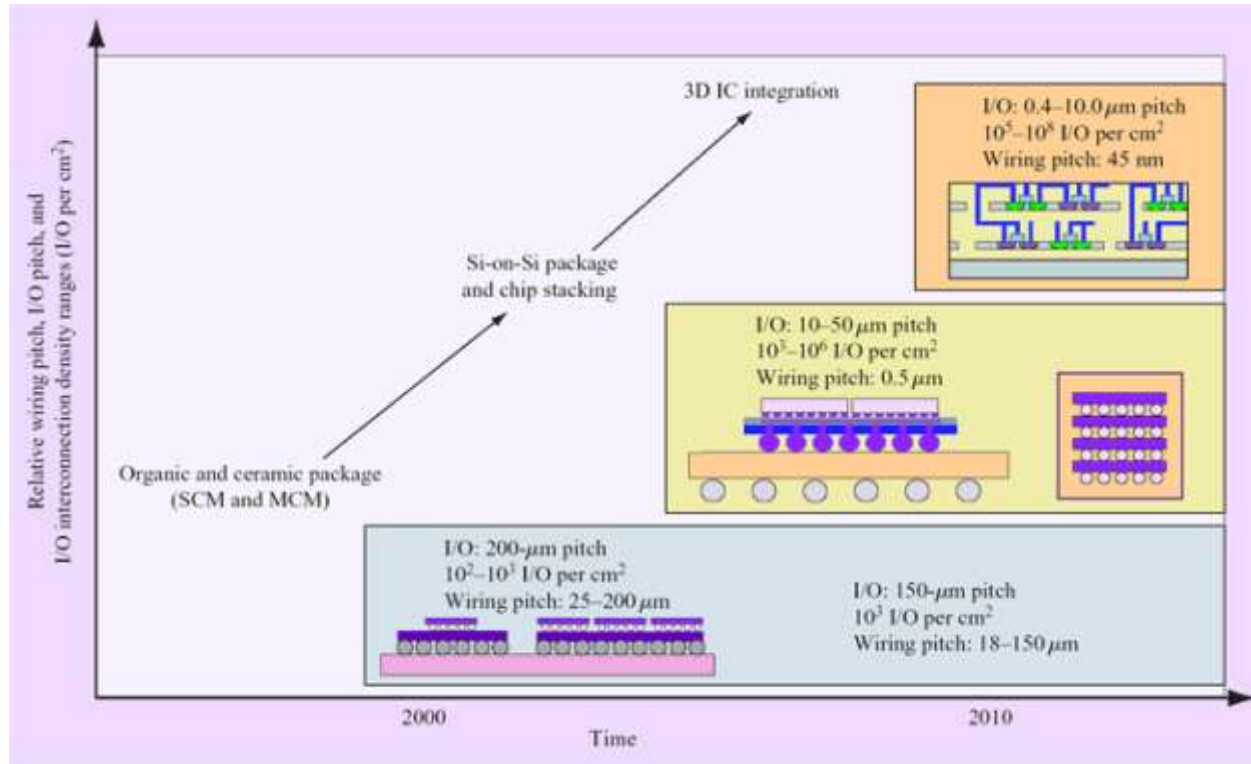


Fig.4 SEM cross sectional photograph and schematic drawing of planarized tripply-stacked IC structure.



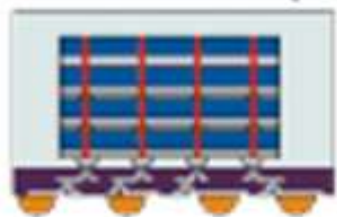
Source IBM <http://www.research.ibm.com/journal/rd/526/knickerbocker.html>

- Moore's law by scaling conventional CMOS involves huge investments.
- 3D IC processes : An opportunity for another path towards continuing the scaling, involving less investments.
- Like for conventional CMOS, infrastructures are needed to promote 3D-IC integration, making it available for prototyping at "reasonable" costs.

Two Worlds with Different Integration Approaches

“Monolithic”

Distributing a whole system across several tiers



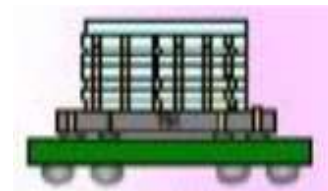
3D-IC TSV Stacked Memory



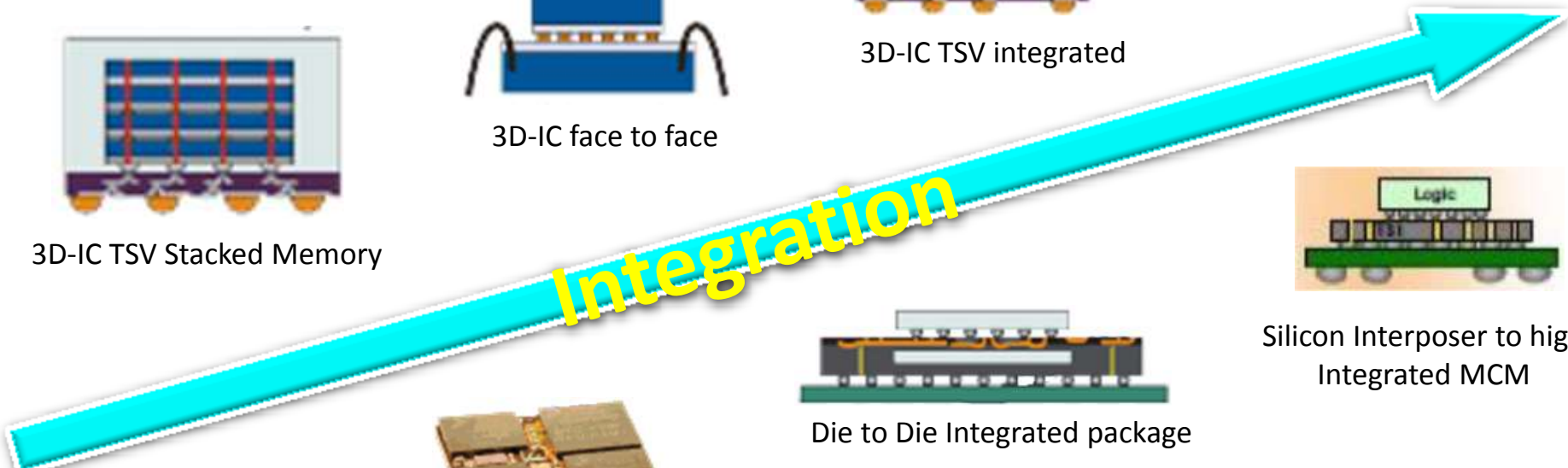
3D-IC face to face



3D-IC TSV integrated



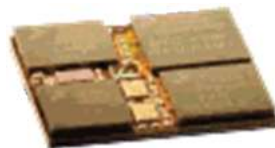
Heterogeneous Multi layer 3D-IC TSV integrated



Integration



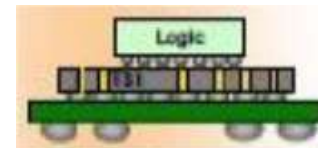
Substrate based Module (PCB)



Multi-Chip Module



Die to Die Integrated package



Silicon Interposer to high Integrated MCM

“Discrete”

Assembly of “Known Good Dies”

Which Design Methodology ?

- Discrete : **3D packaging, stacked dies, ...**

- 1- Design a whole system.

- 2- Split it in subsystems.

- 3- Place the subsystems as predefined “Known Good Dies” (IPs).

- 4- Determine and place the interfaces in between.

- 5- The system is done

- Monolithic : **3D-IC Integration**

- 1- Design a whole system.

- 2- Split it in subsystems.

- 3- Determine and place the interfaces in between.

- 4- Generate and Place the subsystems in between the interfaces.

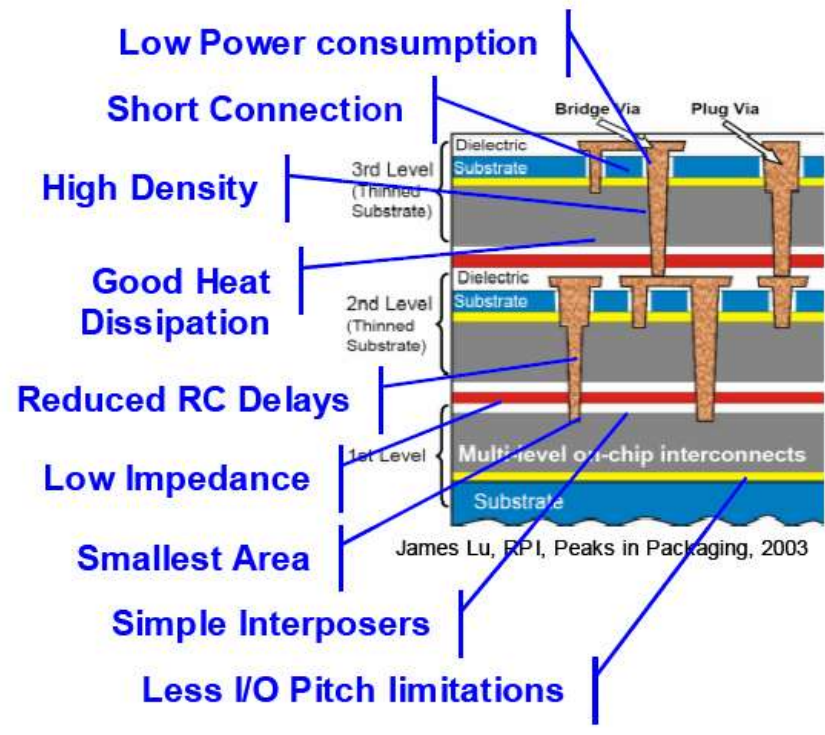
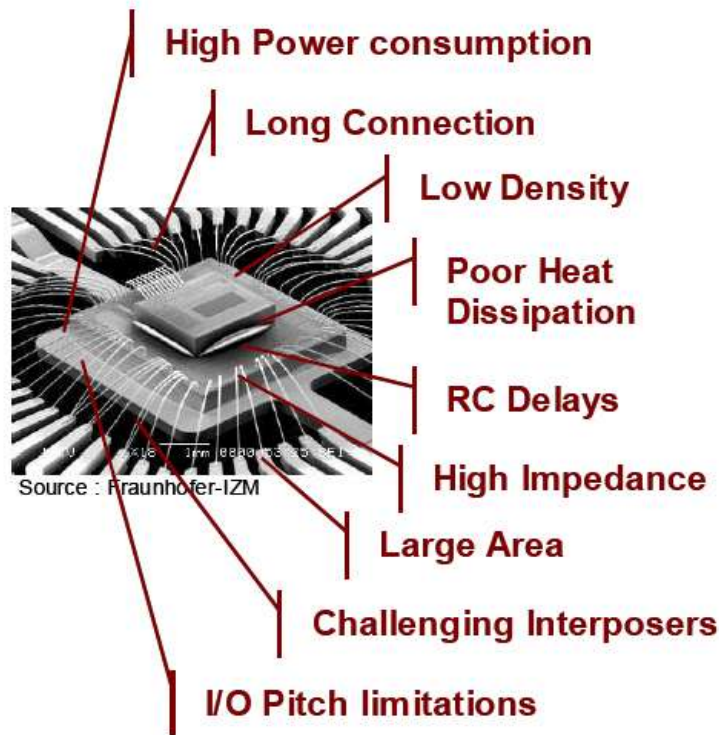
- 5- The system is done

Here comes the difference : The “key” for a true 3D-IC Integration

SiP versus 3D-IC

Why TSV Interconnection?

TSV (Through-Silicon-Via) electrodes can provide vertical connections that are both the shortest and the most plentiful.



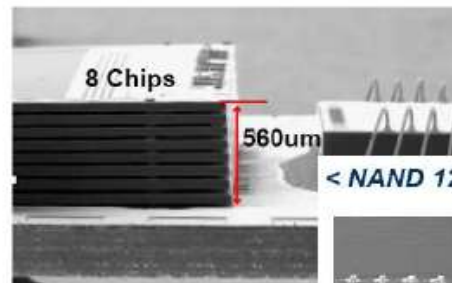
TSV interconnects provide solutions to many limitations of current SiP and Chip Stacking methods.

3D-IC Applications

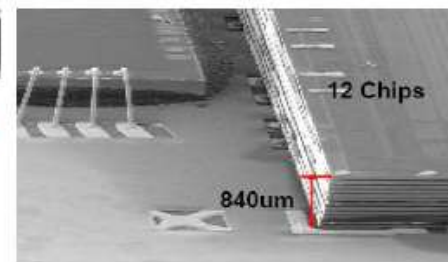
Industrial Applications

- There are two 3D areas that are receiving a lot of attention.
 - Stacked memory chips and memory on CPU
 - IBM expected to provide samples later this year
 - Both IBM and Samsung could be in production next year (2008)
 - Imaging arrays (pixelated devices)
 - Working devices have been demonstrated by MIT LL, RTI, and Ziptronix
 - Much work is supported by DARPA
- Pixel arrays offer the most promise for HEP projects.

< NAND 8 Stacked Memory Card >

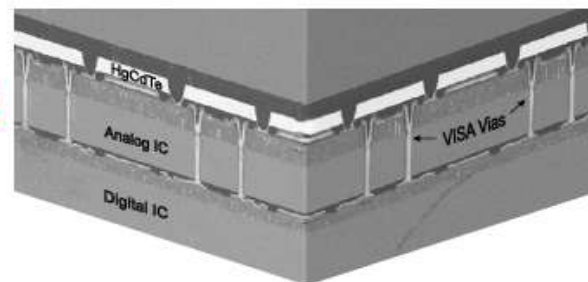


< NAND 12 Stacked Memory Card >



Samsung - 30 um laser drilled vias in 70um chips

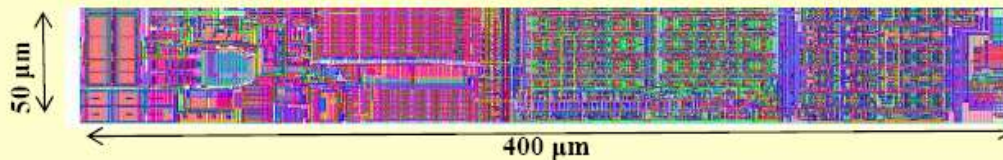
RTI
Infrared
Imager



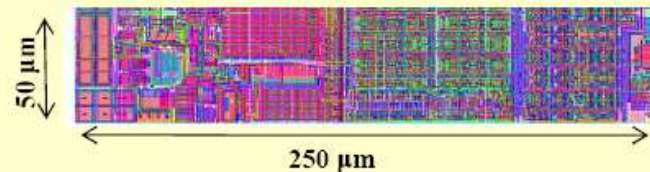
LHC-ILC Workshop on 3D
Integration Techniques

Expected feedback from 3D for SLHC

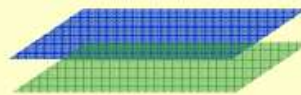
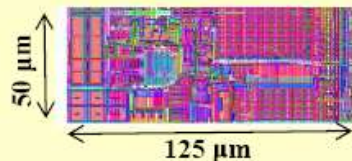
ATLAS Pixel Front End size



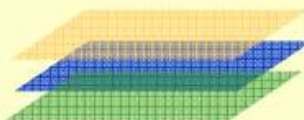
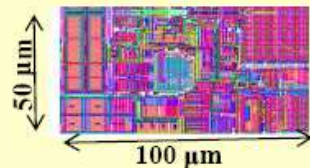
FE-I3 CMOS 250 nm



FE-I4 CMOS 130 nm



FE-I4-3D-2 CMOS 130 nm 2 layers

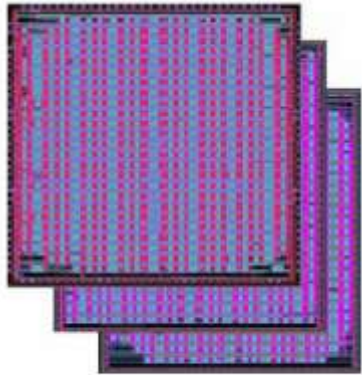


FE-I4-3D-3 CMOS 130 nm 3 layers

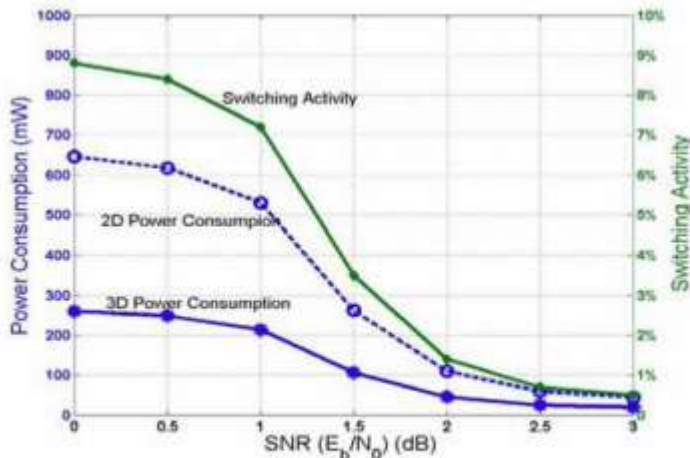
"Implementing a 2-Gbs 1024-bit 1/2-rate Low-Density Parity-Check Code Decoder in Three-Dimensional Integrated Circuits"

Lili Zhou, Cherry Wakayama, Robin Panda, Nuttorn Jangkrajang, Bo Hu, and C.-J. Richard Shi
University of Washington

International Conference on Computer Design, ICCD, Oct. 2007



Final layout view of 3D LDPC structure.



Post-layout power of the LDPC decoder (2D vs 3D).

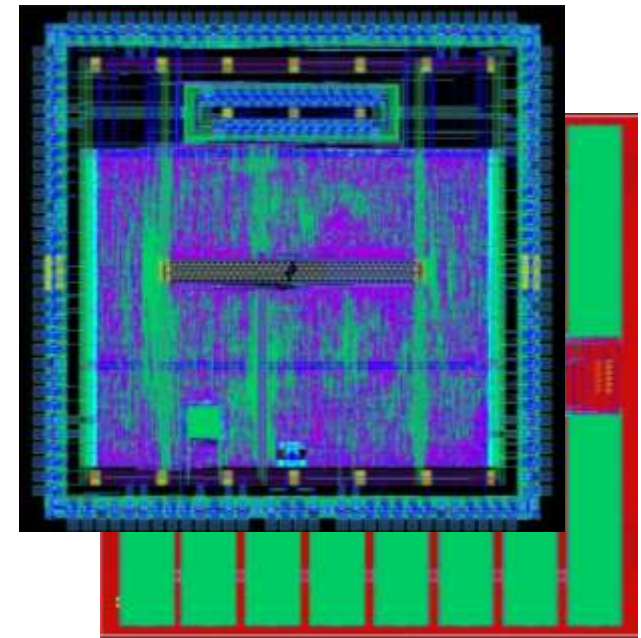
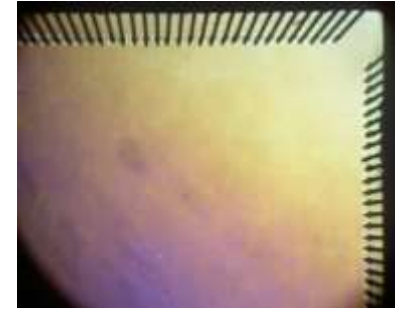
Comparison between 3D and 2D designs

| | 2D design | 3D design |
|-------------------------------------|---------------------------------|-------------------------------------|
| Area (mm*mm) | 18.238*15.92 = 290.35 | (6.4*6.227)*3 = 119.56 |
| Total wire length (m) | 182.42 | 22.39+22.57+22.46 = 67.42 |
| Max WL before buffer insertion (mm) | 13.82 | 8.68 |
| Max WL after buffer insertion (mm) | 4 | 4 |
| Buffer used | 32900 | 24636 |
| Clock skew (ns) | 2.33 | 1 |
| Power dissipation (mw) | 646.2 | 260.2 |

Performance Factor (Area * Timing * Power) = 14

An Illustration: CPU/Memory Stack

- R8051 CPU
 - 80MHz operation; 140MHz Lab test (VDD High)
 - 220MHz Memory interface
 - IEEE 754 Floating point coprocessor
 - 32 bit Integer coprocessor
 - 2 UARTs, Int. Cont., 3 Timers, ...
 - Crypto functions
 - 128KBytes/layer main memory
-
- **5X performance**
 - **1/10th Power**



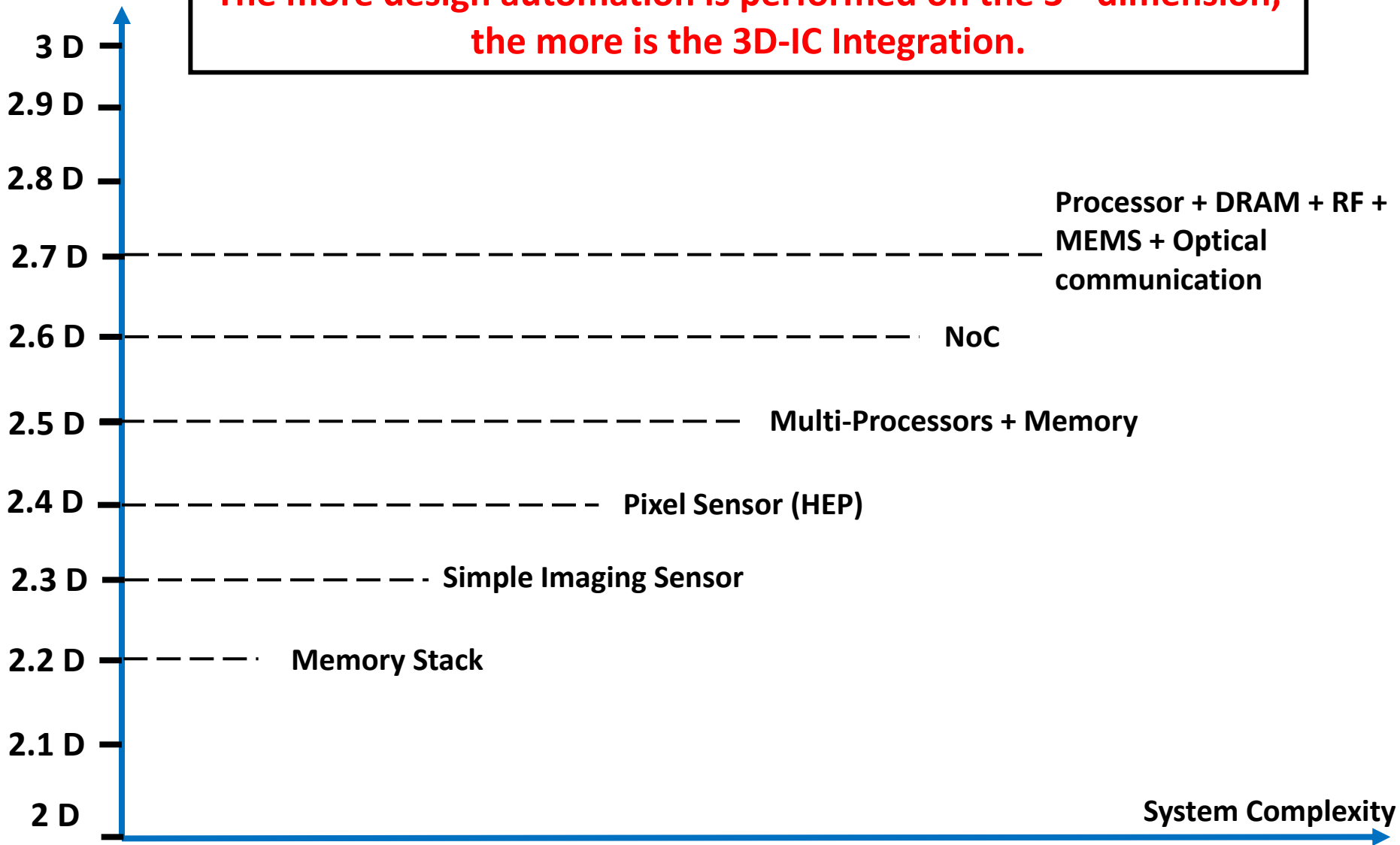
Source Tezzaron (2004)

Some 3D-IC Applications

- **Pixel array for Particle detection (HEP community)**
(Pixel sensor + Analog + Digital + Memory + high speed I/Os)
- **CMOS Image Sensor (Sensor + Processor + Memory)**
- **3D stacked Memories (Flash, DRAM, etc...)**
- **Multi-cores Processor + Cache Memory**
- **NoC (Network on Chip)**
- **Processor + DRAM + RF + MEMS + Optical communication + ...**

Design Methodology

The more design automation is performed on the 3rd dimension, the more is the 3D-IC Integration.

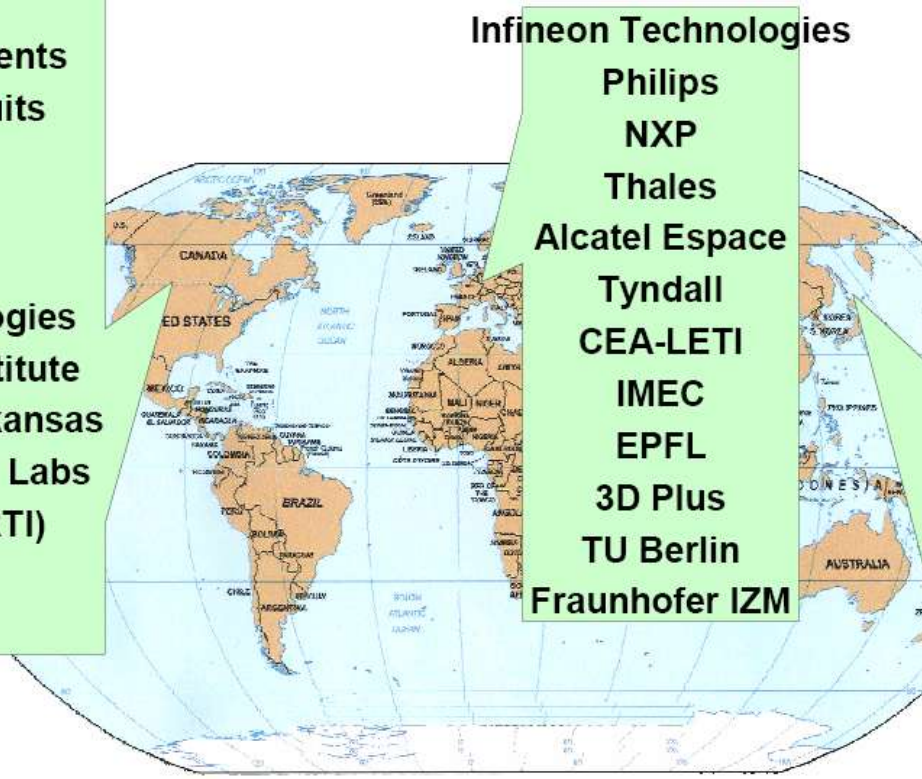




CMC-CMP-MOSIS Collaboration

Global Activities in 3D Integration

Irvine Sensors
 IBM
 Intel
 Texas Instruments
 Vertical Circuits
 Amkor
 Tessera
 Tezzaron
 Tru-Si Technologies
 Rensselaer Institute
 University of Arkansas
 Sandia National Labs
 MCNC-RDI (RTI)
 MIT
 Ziptronix



Infineon Technologies

Philips
 NXP
 Thales
 Alcatel Espace
 Tyndall
 CEA-LETI
 IMEC
 EPFL
 3D Plus
 TU Berlin
 Fraunhofer IZM

ASET
 NEC
 Tohoku University
 University of Tokyo
 ZyCube
 CREST
 Fujitsu
 Sanyo
 Sony
 Toshiba
 Denso
 Mitsubishi
 Sharp
 Hitachi
 Matsushita
 Samsung

CMC / CMP / MOSIS partnering for 3D-IC process access

- **Stimulate the activity by sharing the expenses for manufacturing.**
- **Join forces for the technical support, and dedicate the roles for each partner.**
- **Make easier the tech support for local users respectively by each local center.**
- **Because there is no standard for the 3D-IC integration, it is urgent to setup an infrastructure making possible a broad adoption of 3D-ICs. That will have a beneficial effect on prices, more frequent MPW runs, and more skilled engineers.**



CNRS - INPG - UJF

CMC-CMP-MOSIS partnering on 3D-IC



CMP/CMC/MOSIS partner to introduce a 3D-IC process

Grenoble, France, 22 June 2010, CMP/CMC/MOSIS are partnering to offer a 3D-IC

MPW service based on Tezzaron's SuperContact technology and GLOBALFOUNDRIES 130nm CMOS.

The first MPW run is scheduled to 31 May 2011:

- 2-tier face-to-face bonded wafers
- 130nm CMOS process for both tiers
- Top tier exposing TSV and backside metal pads for wire bonding.

A design-kit supporting 3D-IC design with standard-cells and IO libraries is available.

Further MPW runs will be scheduled supporting process flavors (multiple tiers beyond 2, different CMOS flavors for different tiers, ...) driven by user requirements.

Potential users are encouraged to contact **CMP** for details : cmp@imag.fr

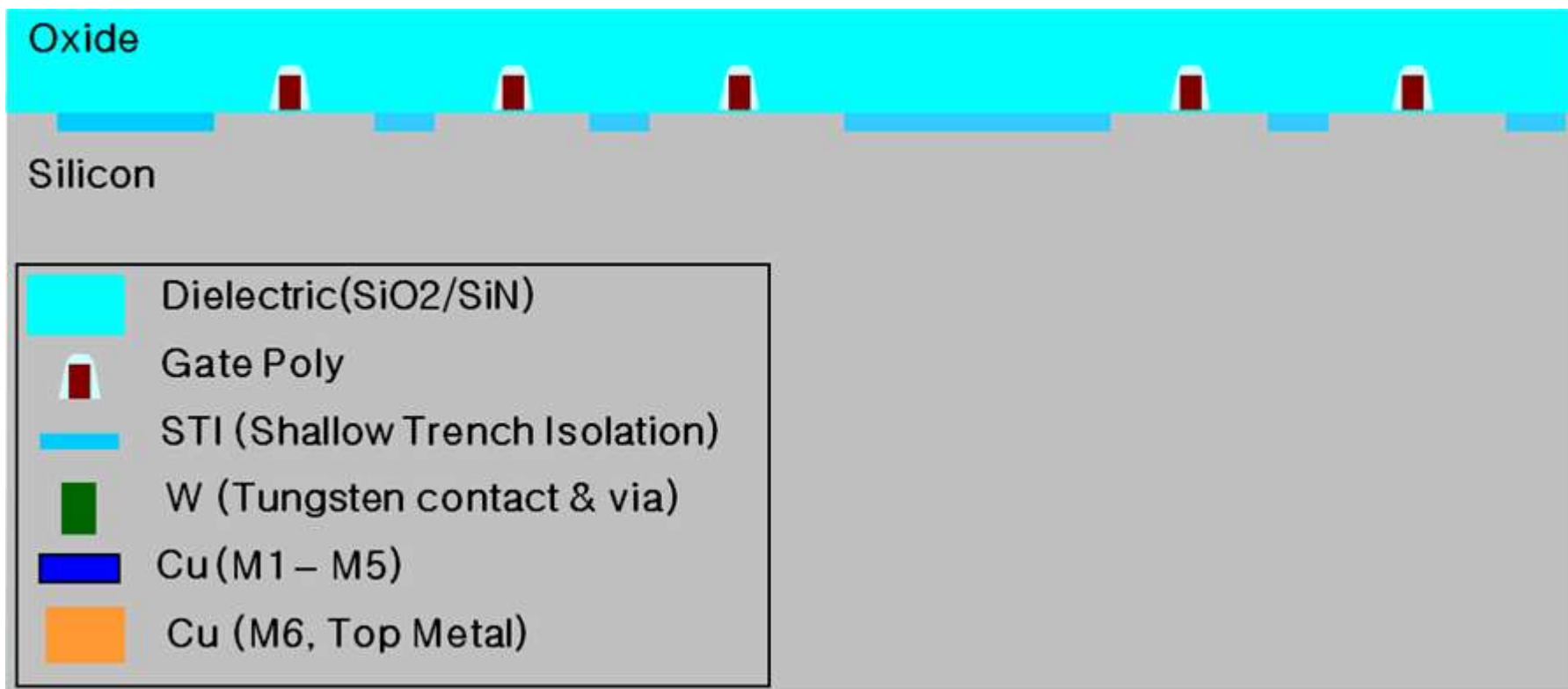
CMC - CMP - MOSIS Cooperation

- CMC supporting Canadian Customers
- CMP supporting European Customers
- MOSIS supporting US Customers
- Each may support other locations



Tezzaron 2-Tier Process (130nm CMOS)

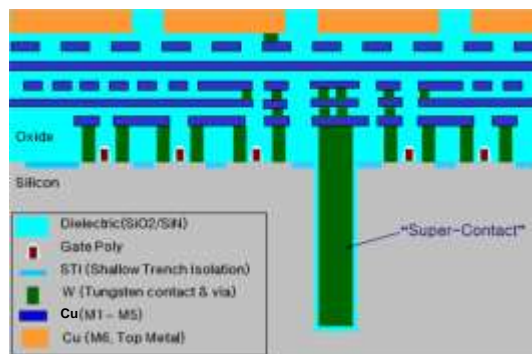
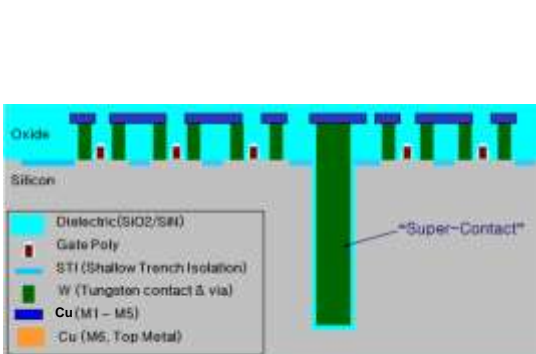
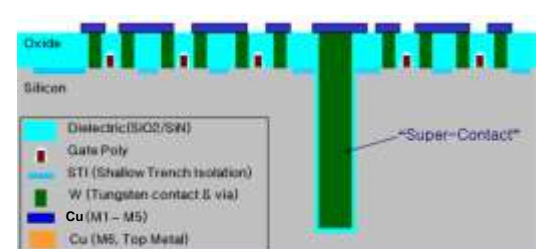
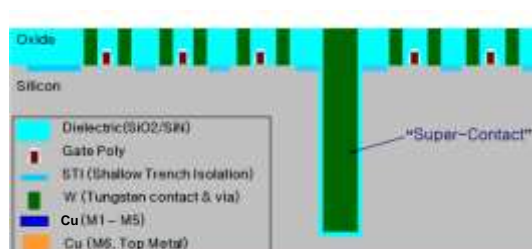
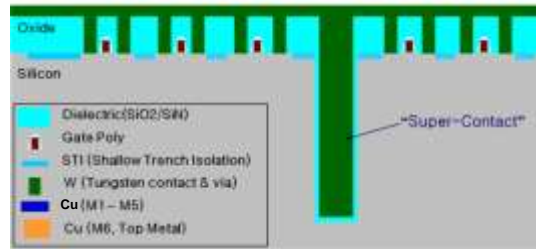
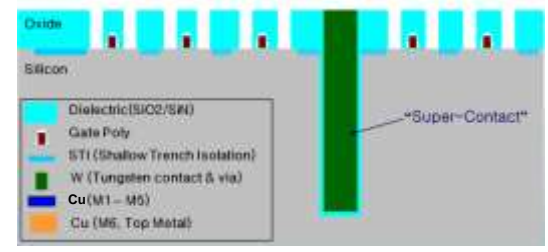
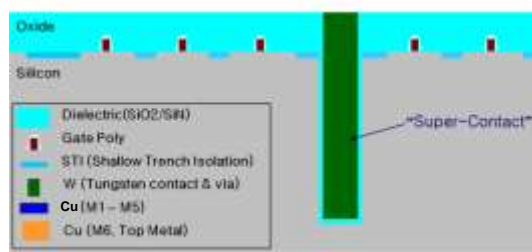
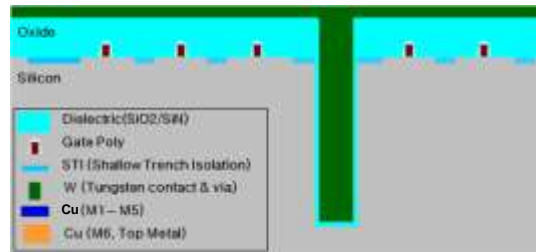
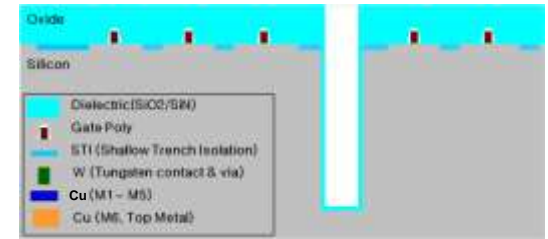
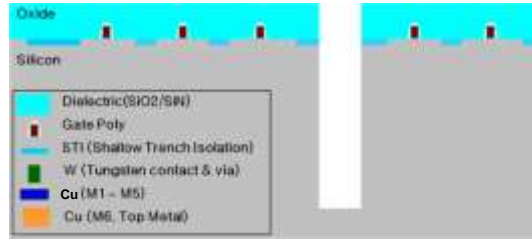
Process Overview

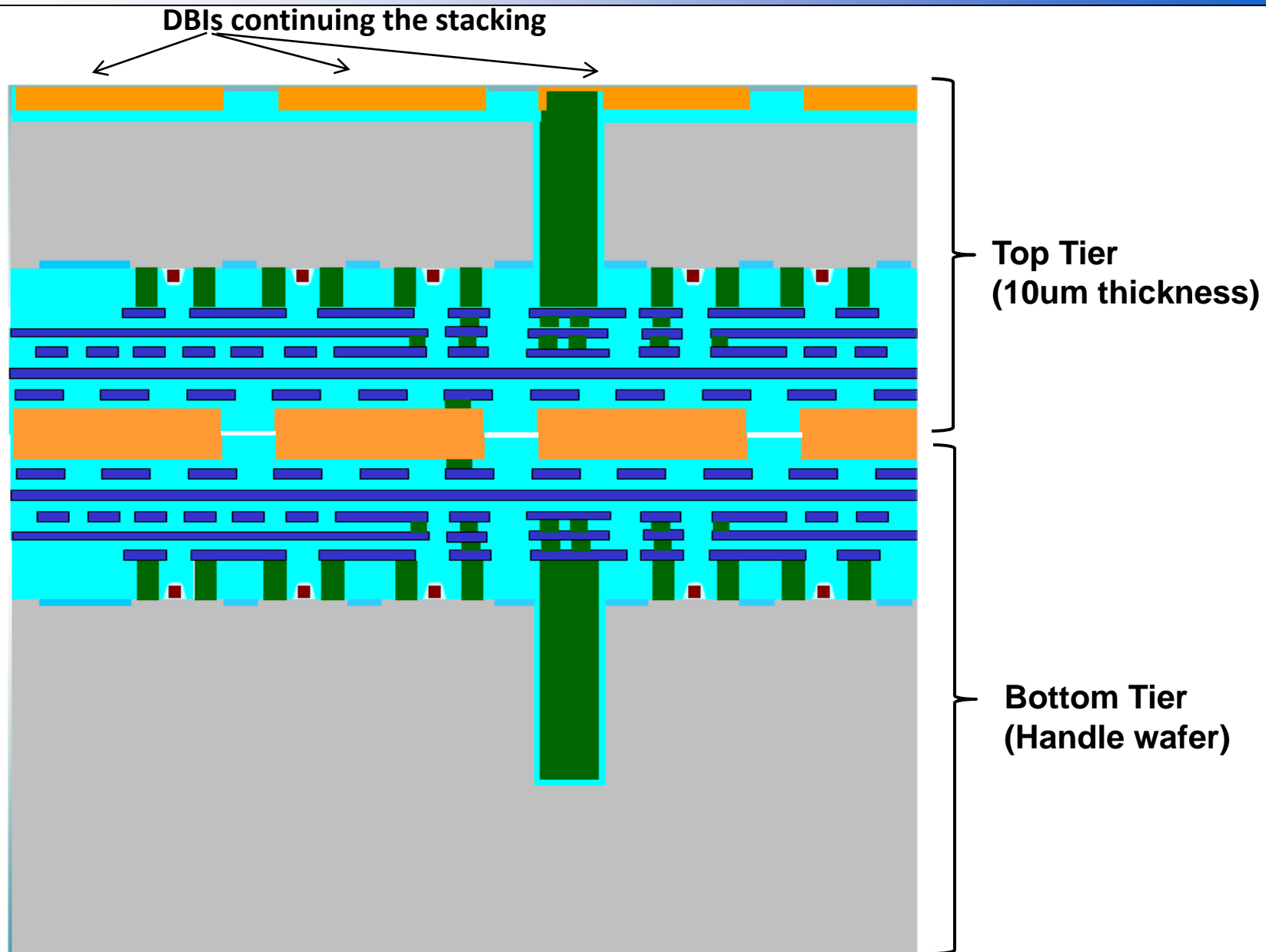


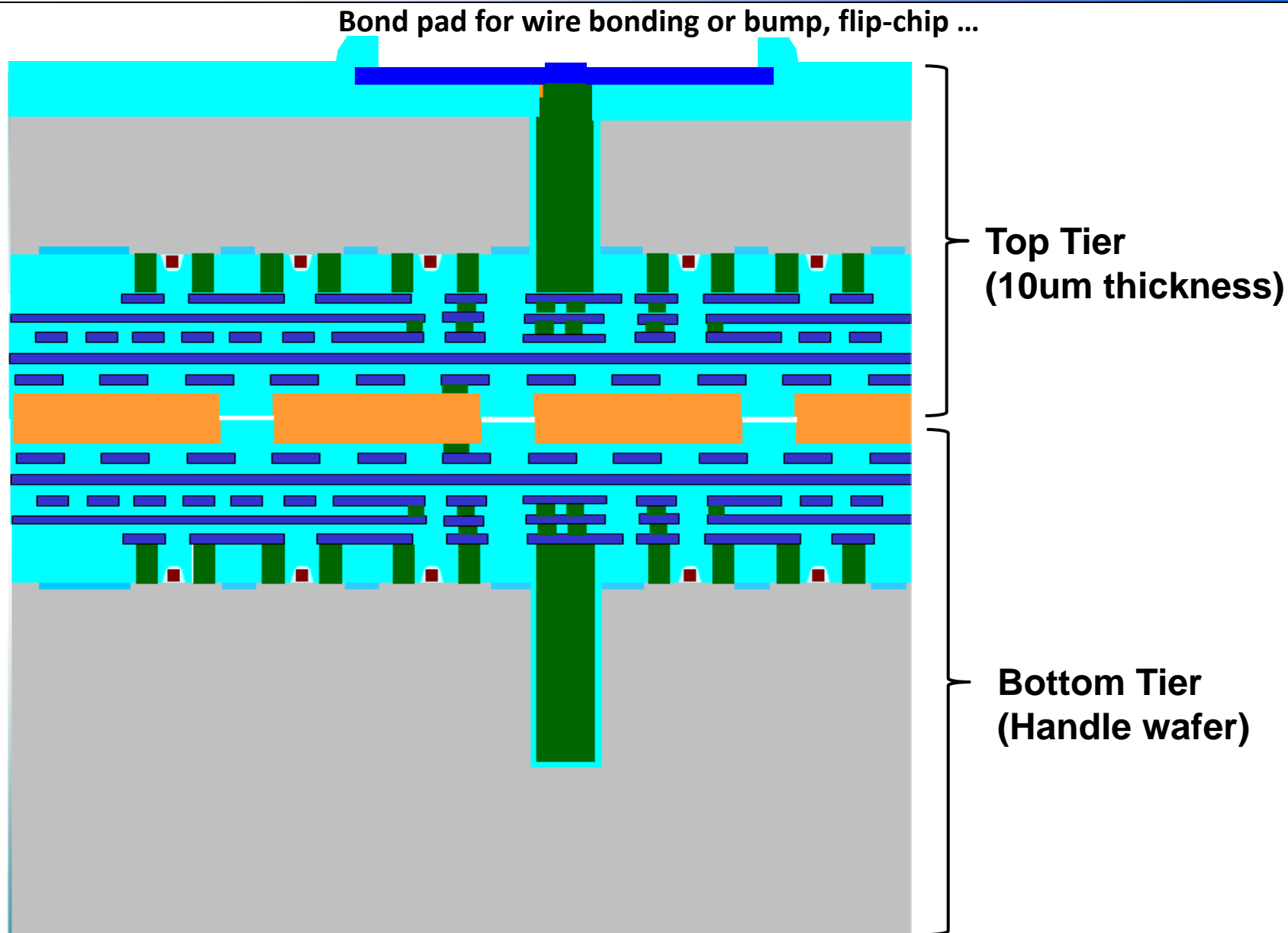
Starting wafer in 130nm (5 Cu metal layers + 6th Cu metal as DBI)

Source Tezzaron

Tezzaron Process Flow for TSV and DBI (using Via Middle process)



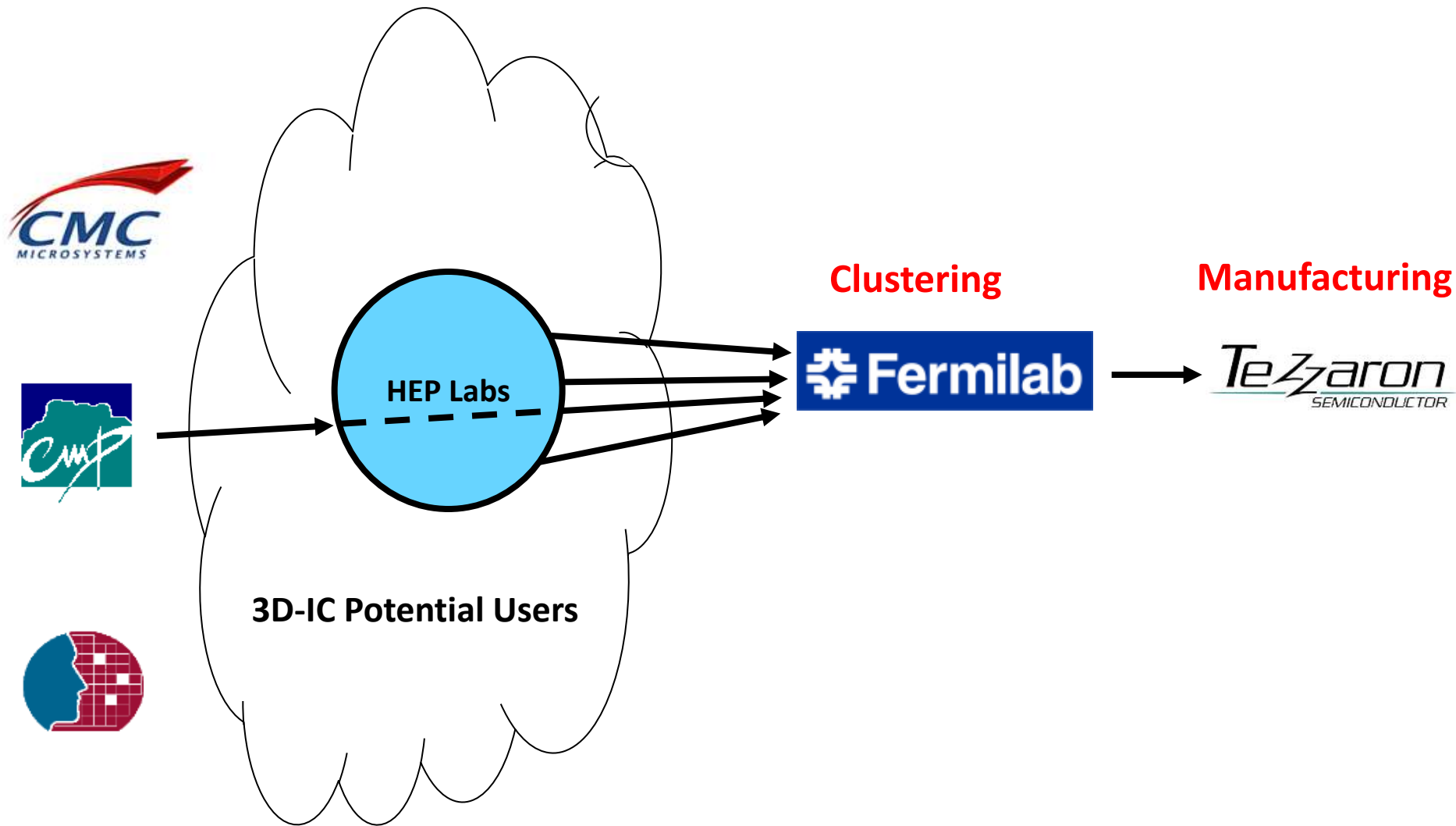




3D-IC MPW runs

3D-IC MPW Initial Infrastructure

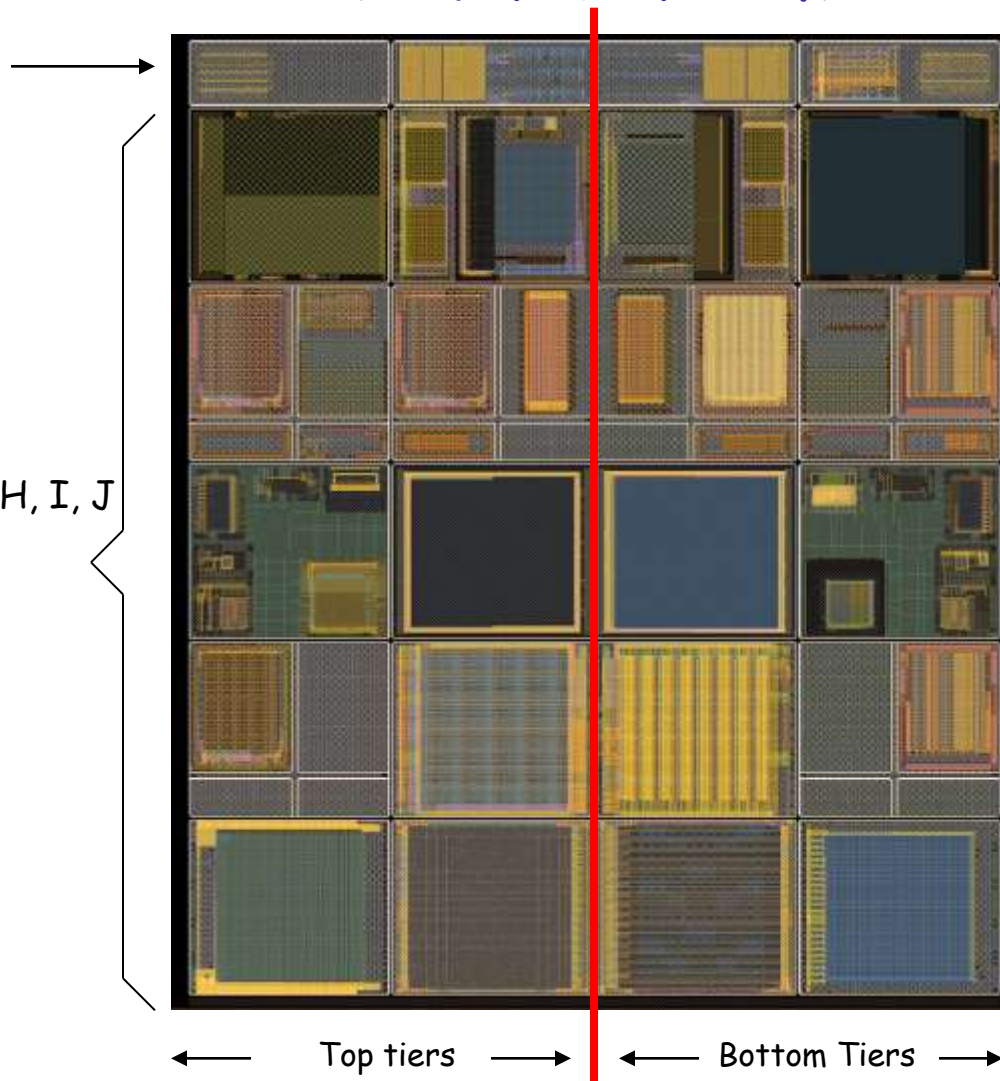
First MPW Run organized by FermiLab using an Industrial Process



MPW Full Frame

Test chips:
TX, TY
2.0 x 6.3 mm

Subreticules:
A, B, C, D, E, F, G, H, I, J
5.5 x 6.3 mm

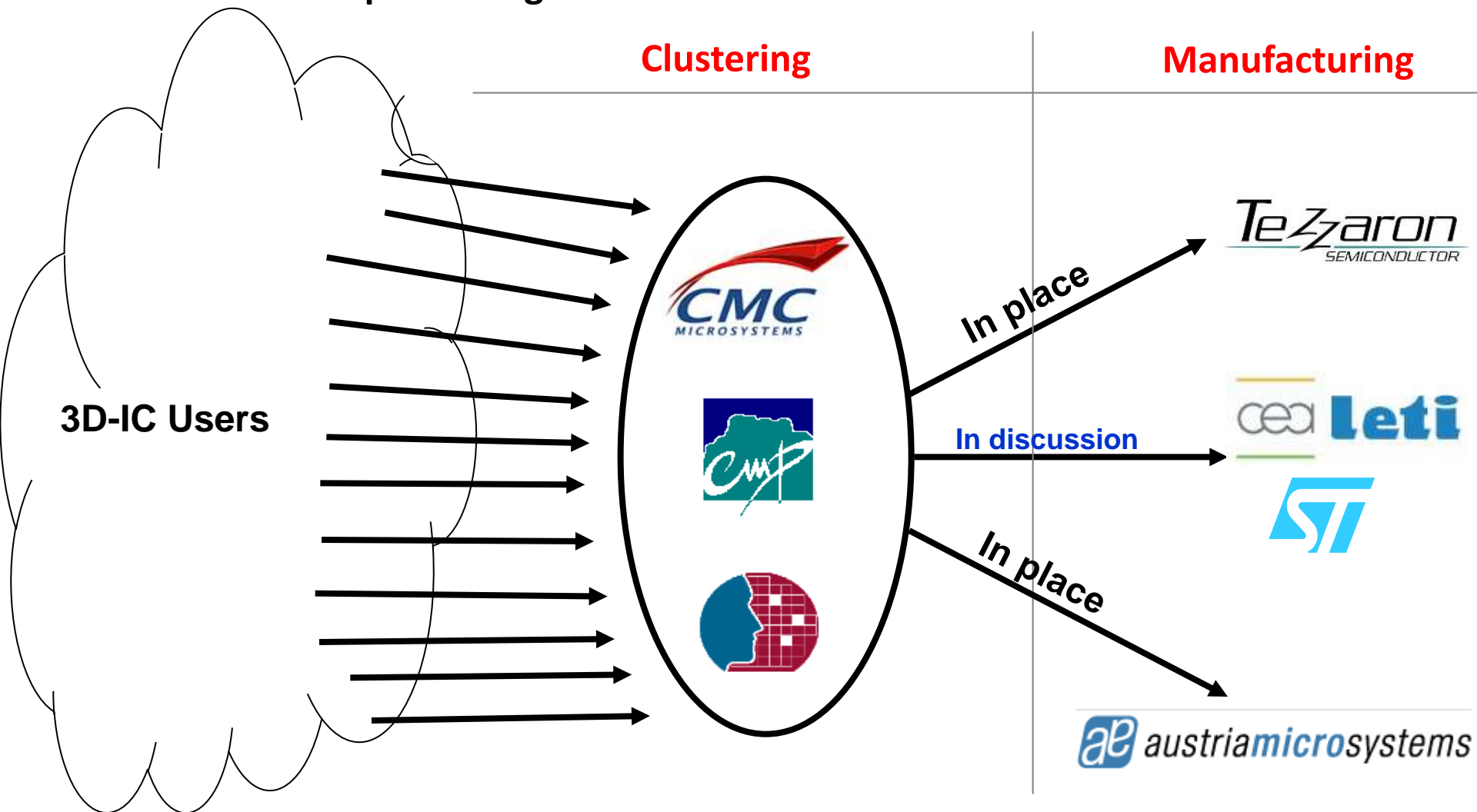


Notice
Symmetry
about vertical
center line

Source FermiLab (3D Consortium Meeting)

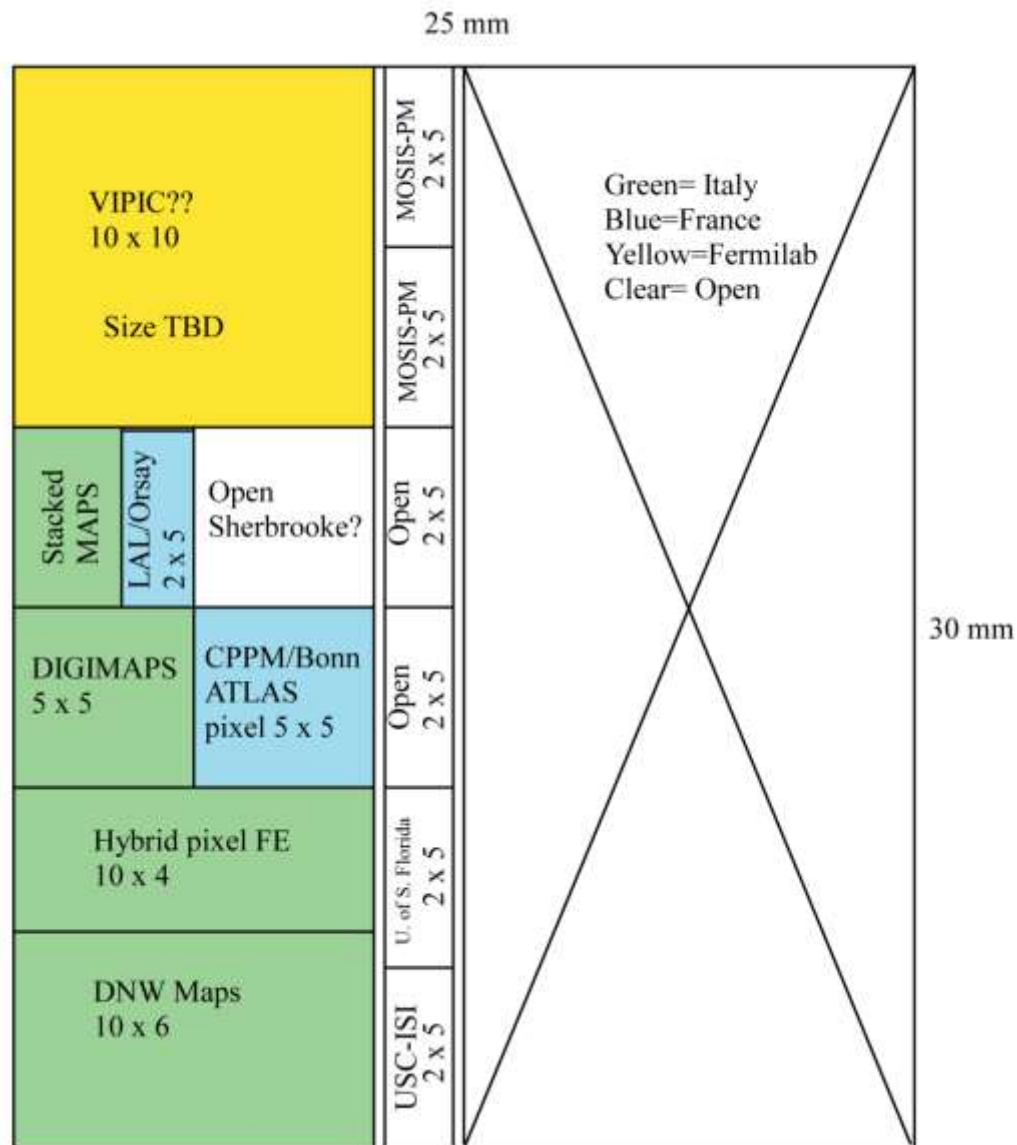
3D-IC MPW Infrastructure

CMC-CMP-MOSIS partnering to offer 3D-IC MPW runs



Critical mass will allow frequent MPW runs and low pricing

CMP/MOSIS/CMC : 1st MPW run



MPW run deadline : May 31st, 2011

3D-IC Design Platform

- A common root installation for the different parts of the Design Platform
 - **PDK**
 - **Libraries**
 - **Memory compilers**
 - **Utilities**
 - **Tutorials**
- Defining a unique variable for the root installation.
All the modules inside refer to this unique variable.



Making the Design Platform portable to any site.

Collaborative Work to the Design Platform

HEP labs contributing with Programs, Libraries, and Utilities. All included in the Design Platform

- DBI (direct bonding interface) cells library. (FermiLab)
- 3D Pad template compatible with the ARM IO lib. (IPHC)
- Preprocessor for 3D LVS / Calibre (NCSU)
- Skill program to generate an array of labels (IPHC)
- Calibre 3D DRC (Univ. of Bonn)
- Dummies filling generator under Assura (CMP)
- Basic logic cells and IO pads (FermiLab)
- Floor-planning / automatic Place & Route using DBIs, and TSVs (CMP)
- Skill program generating automatically sealrings and scribes (FermiLab)
- MicroMagic PDK (Tezzaron/NCSU)



Virtuoso Layout Editor with 3D layers and verification

CNRS - INPG - UJF

- TSV →
 - Back Metal →
 - Back Pad →
 - DBI →
- | | |
|-------------|-----|
| NO_FILL | drw |
| TSCSuperCnt | drw |
| TSCBackMet0 | drw |
| TSCBackMet0 | lbl |
| TSCBackMet1 | drw |
| TSCBackMet1 | lbl |
| TSCBPad | drw |
| SRAM_TSC | drw |
| PR_BNDRY | drw |
| NWELL | drw |
| DNWELL | drw |
| LDMOS_XTOR | mar |
| COMP | drw |
| POLY2 | drw |
| POLY2 | lbl |
| PPLUS | drw |
| NPLUS | drw |
| CNT | drw |
| MET1 | drw |
| MET1 | lbl |
| VIA1 | drw |
| MET2 | drw |
| MET2 | lbl |
| VIA2 | drw |
| MET3 | drw |
| MET3 | lbl |
| VIA3 | drw |
| MET4 | drw |
| MET4 | lbl |
| VIA4 | drw |
| MET5 | drw |
| MET5 | lbl |
| VIATOP | drw |
| METTOP | drw |

X: 12.500 Y: -4.115 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 2

Tools Design Window Create Edit Verify Connectivity Options Routing Assura Calibre Help

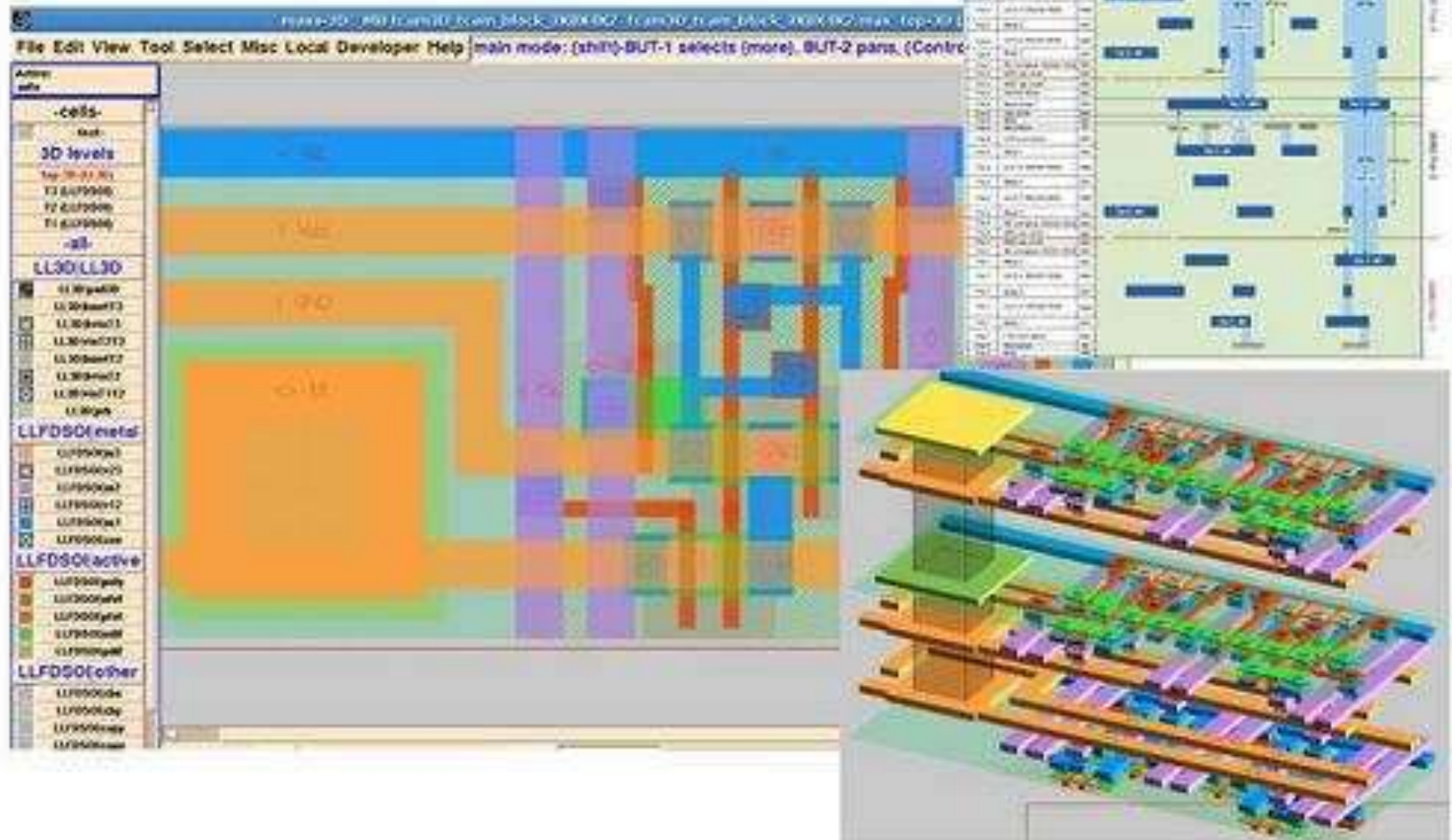
Calibre

Assura

mouse L: mouseSingleSelectPt M: leHiMousePopUp() R: hiZoomAbsoluteScale (hiGetCurrentWi

Technology Files fully supported by Tezzaron

MicroMagic MAX-3D



System Level Partitioning

Design exploration at system level

3D Floor-Planning
DBI, TSV, IO placement

Design exploration at the physical level
DBI, TSV, and IO placement & optimization

Automatic Place & Route

Cells and blocks place & route can be
done tier by tier

Extraction, Timing Analysis

To be done for each tier, then combined for
back-annotation to the 3D top level system

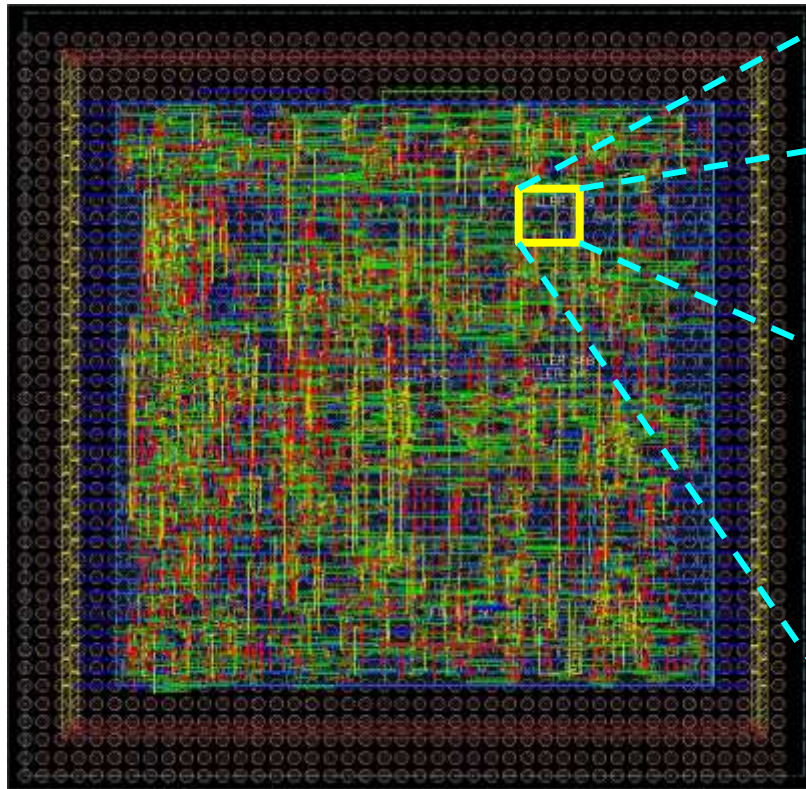
Physical verification
3D DRC, 3D LVS

Dummies Filling

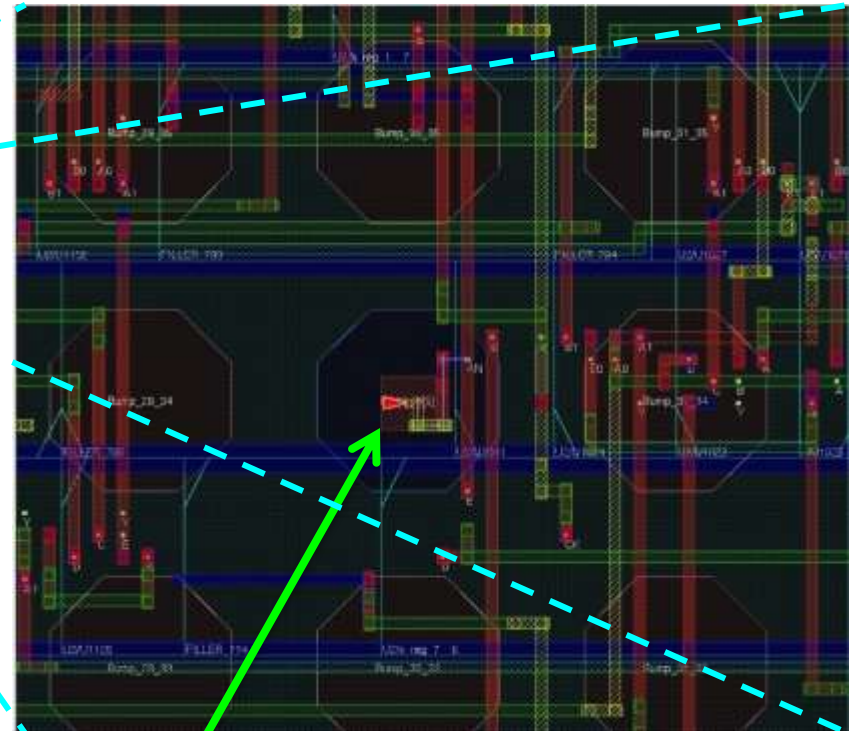
Final 3D DRC

Similar to the full-custom design flow

- Encounter natively refuses to make the routing for pins on DBIs.
- Custom scripts solved the problem. It's a workaround.
- The resulting layout is compliant to the Tezzaron DRC, LVS etc ...



DBI array generation + P&R

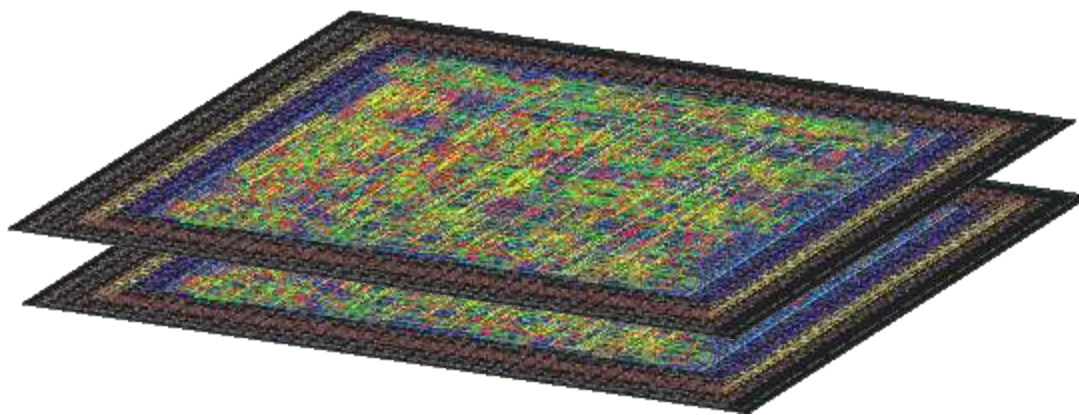


DBI completely routed down to the lower metal layers

Automatic P&R with Direct Bond Interface

Saving the floor plan for the bottom tier, and apply it for top tier so the automatic Place & Route run the placement and routing taking into account the DBI locations.

The place & route for both tiers is optimal for timing, buffer sizing and power performance.



This should result in a **“correct by construction”** design.

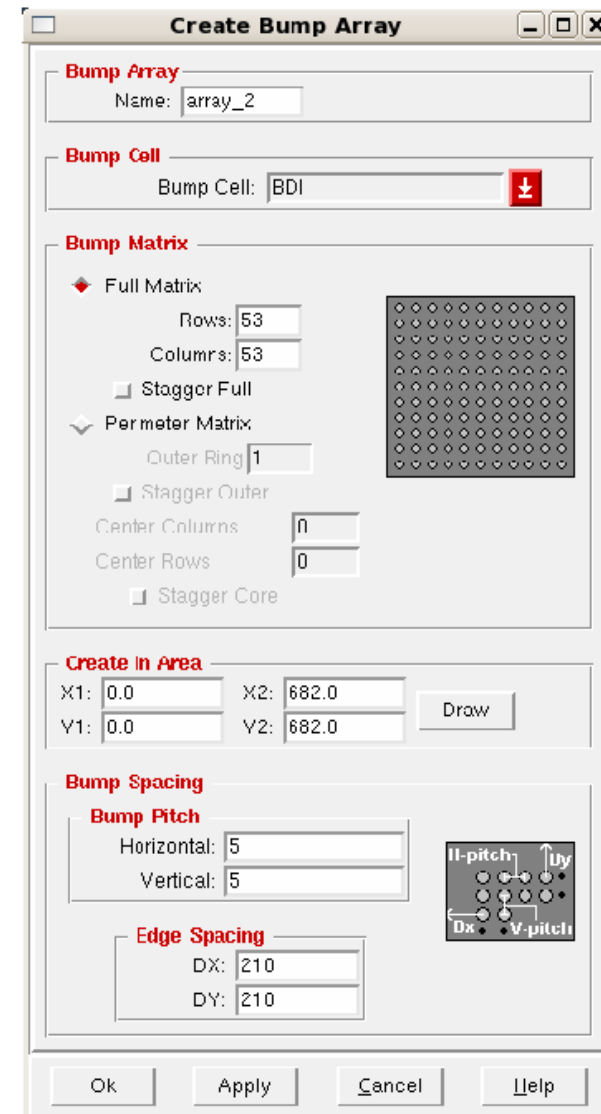
➤ Create Bump Array

Floorplan > Flip Chip > Create bump Array...

Specify the array Name, number of bumps, pitch, ...
Then click OK.

To save an IO file with this bump array choose the following menu:

Design > Save > I/O File...



Cadence / Encounter v 8.1 Signal Bumps Assignment

Floorplan > Flip Chip > Assign Signal...

1. Select the IO signal in the list
2. Select the bump to be assigned
3. Click "Assign". The selected bump become blue.

The screenshot shows the 'Assign/Unassign Signals' dialog box in the foreground, overlaid on the Encounter 8.1 floorplan view. The dialog box contains a 'Signal List' table with columns for IO Signal, Driver, Cell, Pin, Location, Tile/Bump, Tile Pin, and Loc. The signal 'ADC_Convctb' is selected, and its location is '(nu l)'. Below the table, there are options for 'Assign to Tiles/Bumps' (n Select Set, n Created Order, Closest) and 'Set Net Wire Width' (Wire Width: [] Set). The floorplan view in the background shows a grid of bumps, with one bump highlighted in blue, indicating it has been assigned to the selected signal.

| IO Signal | Driver | Cell | Pin | Location | Tile/Bump | Tile Pin | Loc |
|---------------|----------------|------|--------|---------------|------------|----------|---------|
| Filter_In[2] | io_in2 | PIC | P | x=0.0 y=411.0 | | | |
| Filter_In[1] | io_in1 | PIC | P | x=0.0 y=341.0 | | | |
| Filter_In[0] | io_in0 | PIC | P | x=0.0 y=271.0 | | | |
| C_K | io_in_CLK | PIC | P | x=218.5 y=0.0 | | | |
| RESET | io_in_RESET | PIC | P | x=306.0 y=0.0 | | | |
| ADC_Busy | io_in_ADC_busy | PIC | P | x=333.5 y=0.0 | | | |
| ADC_Convctb | (nu l) | | (nu l) | | | | |
| ADC_Rd_csb | (nu l) | | (nu l) | | Bump_22_26 | | x=318.3 |
| Filter_Out[7] | (nu l) | | (nu l) | | Bump_35_33 | | x=363.3 |
| Filter_Out[6] | (nu l) | | (nu l) | | Bump_29_33 | | x=353.3 |
| Filter_Out[5] | (nu l) | | (nu l) | | Bump_23_33 | | x=323.3 |
| Filter_Out[4] | (nu l) | | (nu l) | | Bump_17_33 | | x=293.3 |
| Filter_Out[3] | (nu l) | | (nu l) | | Bump_35_19 | | x=363.3 |
| Filter_Out[2] | (nu l) | | (nu l) | | Bump_29_19 | | x=353.3 |
| Filter_Out[1] | (nu l) | | (nu l) | | Bump_23_19 | | x=323.3 |
| Filter_Out[0] | (nu l) | | (nu l) | | Bump_17_19 | | x=293.3 |

Number of IO Signals: 21

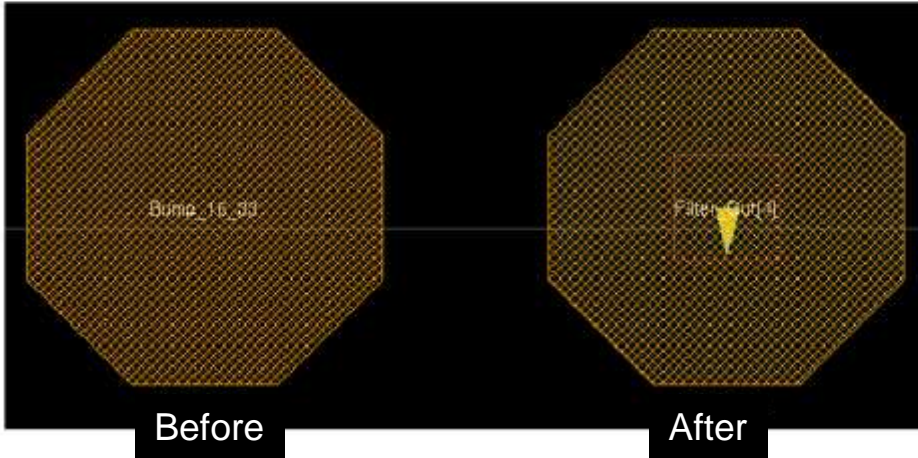
Assign to Tiles/Bumps:
 n Select Set
 n Created Order Set Order: As Is
 Closest

Set Net Wire Width:
 Wire Width: [] Set

Buttons: Assign, Unassign, Done

Create pins under bumps:

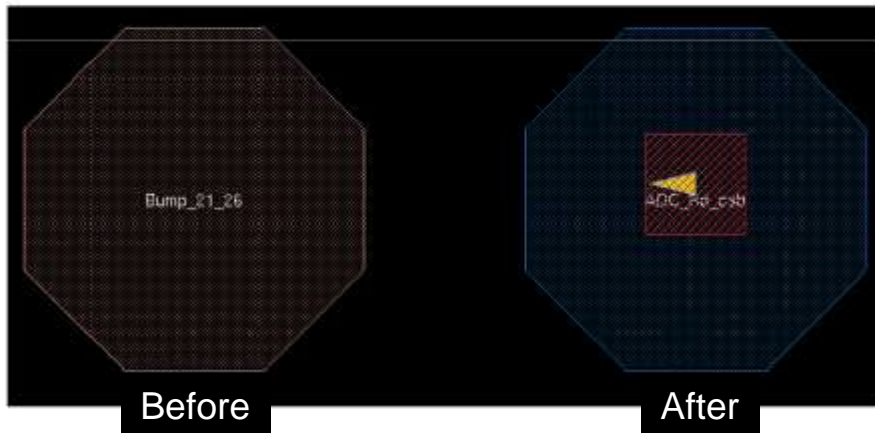
```
exec ../ScriptsBDI/makePhysical_Pins.sed Design_pins_bumps.io makePhyPins.do
```



Placing logical pins on bumps (DBIs), and extract their location.

Generating physical pins under bumps:

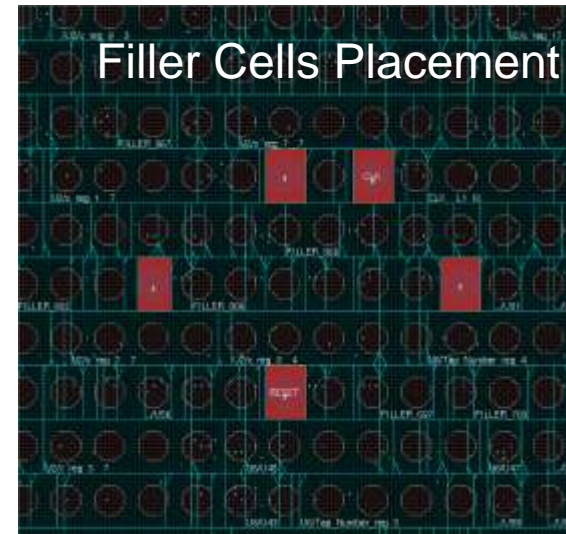
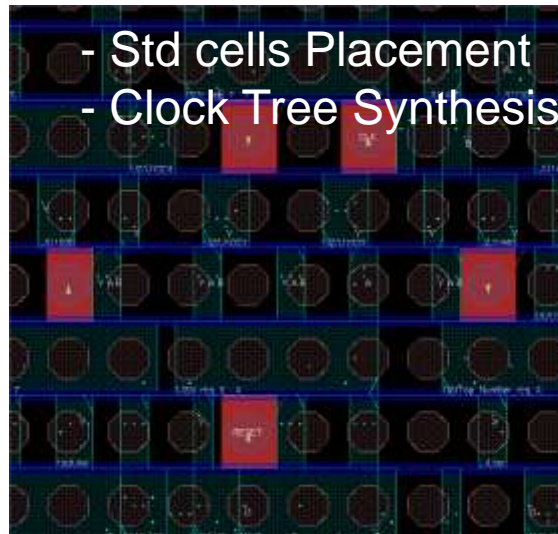
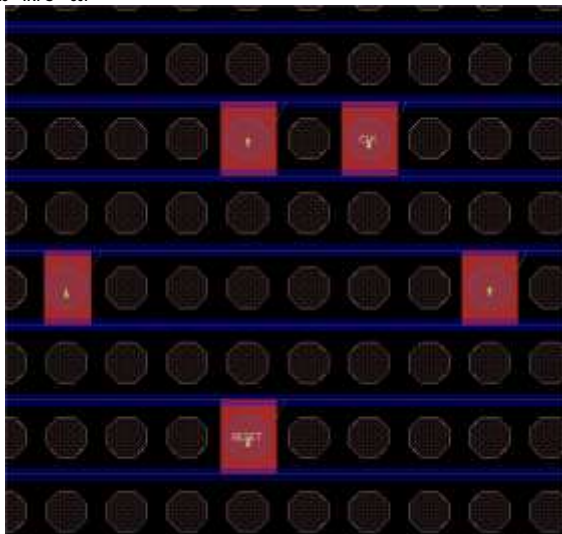
```
source makePhyPins.do
setBumpFixed -allBumps
```



Generating Physical pins from these locations.
They can now be used as terminals for routing.

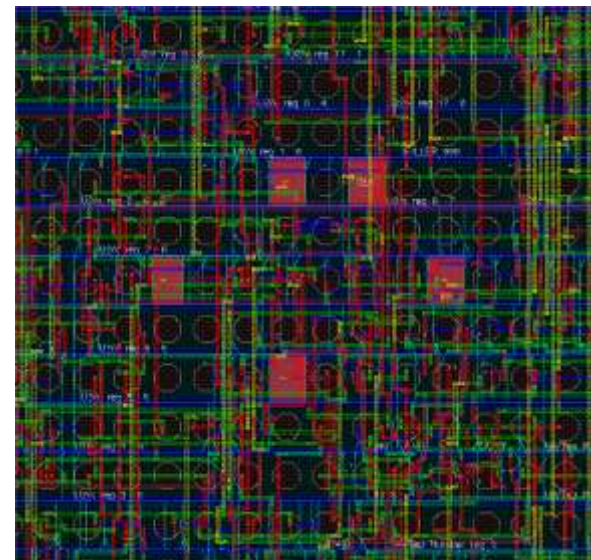
Automatic P & R Design Flow (From Floor-Plan to Routed Design)

CNRS - INPG - UJF



- DBIs Placement
- TSVs Placement
- Obstructions on TSVs

- Clock routing
- Final routing



⚠ The M6 layer must not be used during routing. This layer is reserved for DBI.

➤ Routing Clock Nets

Route > NanoRoute > Route...

Switch **Selected Nets Only** in the *Routing Control* panel.

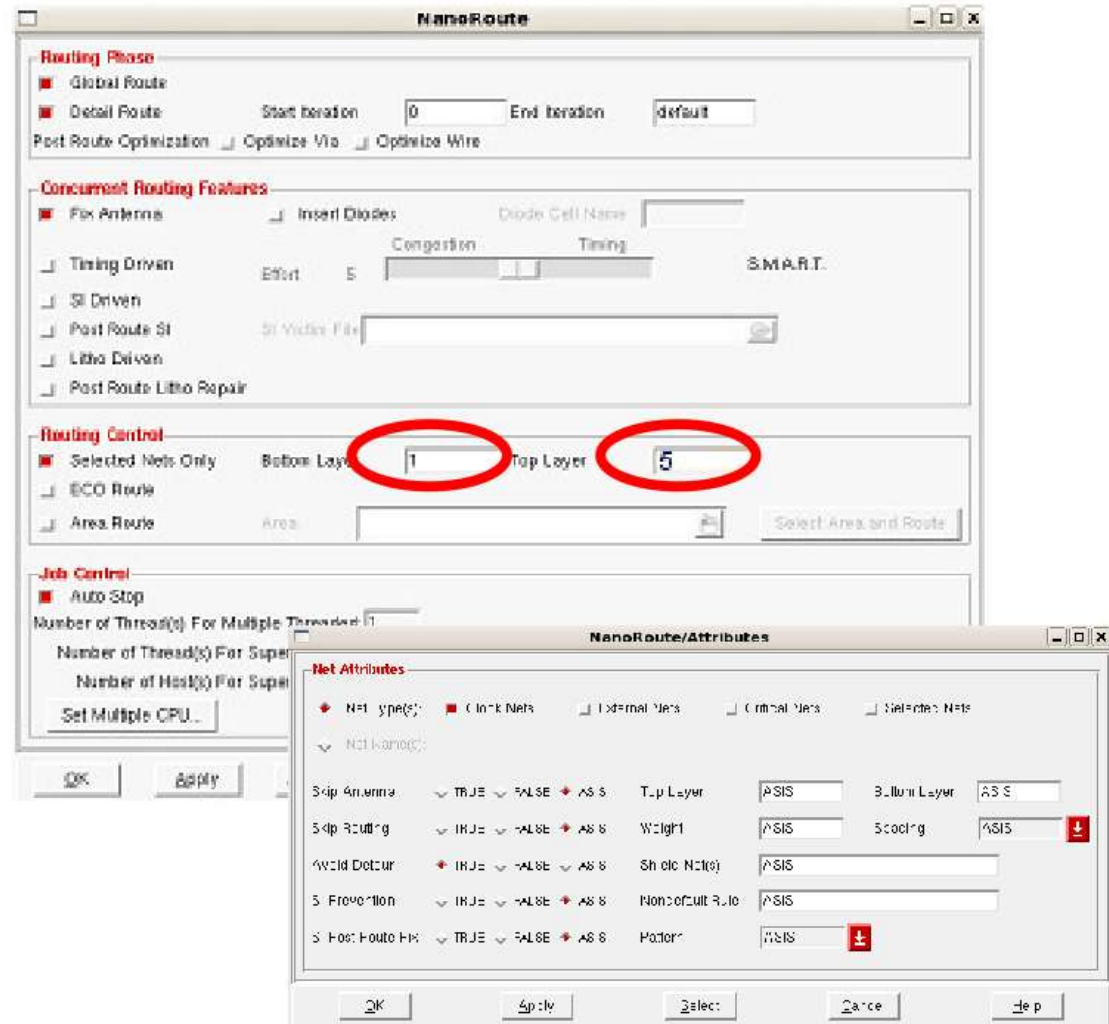
In the **Attribute Menu**, select :
Net Type : **Clock Nets**

Avoid Detour: **True**

(this allows to route the clock nets as straight as possible)

Use the “Mode setup” panel to switch the different options (for example, define the bottom/top routing layer).

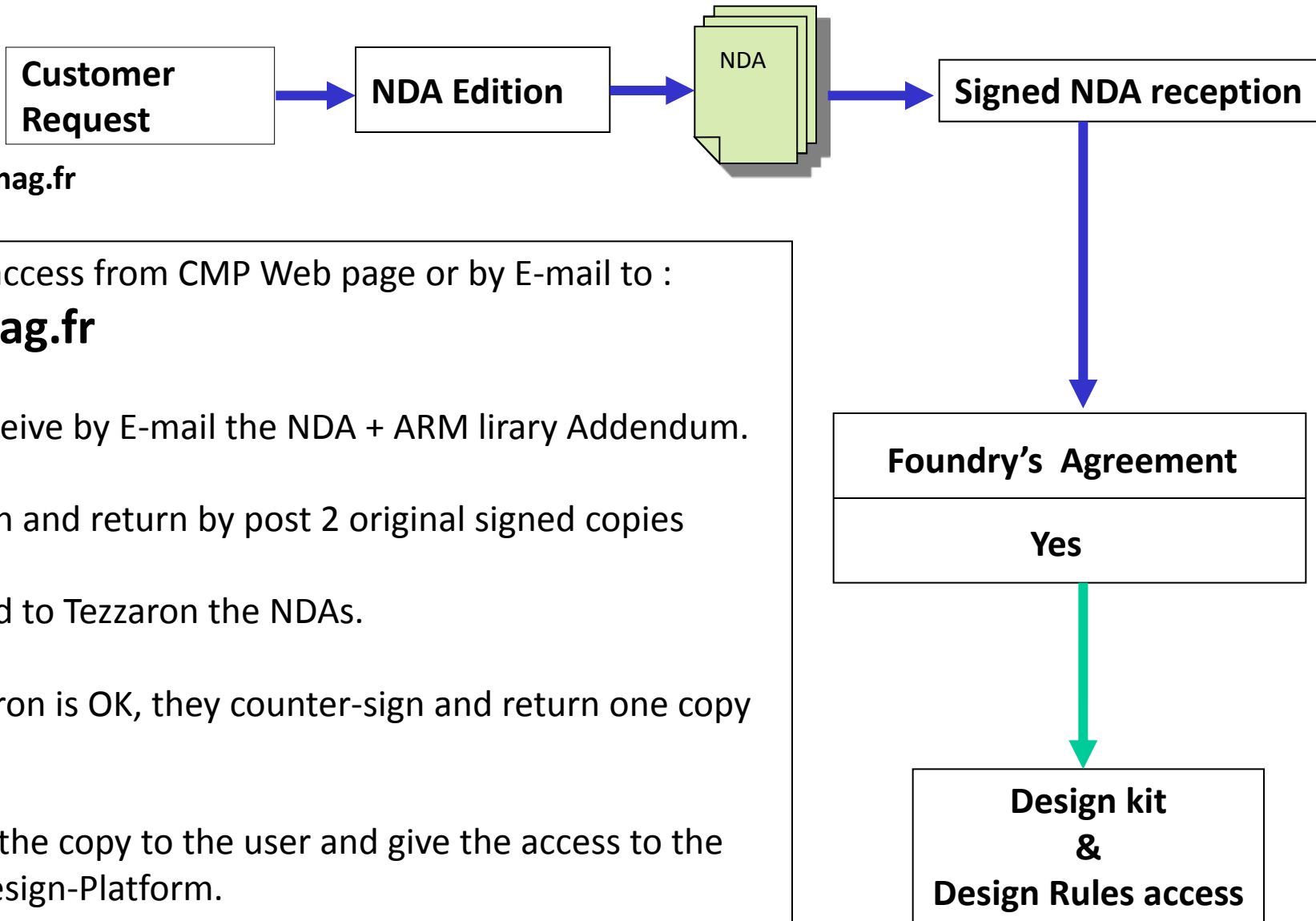
Click OK to run Nanoroute.



Access to the Design-Rules and the Design Platform



<http://cmp.imag.fr>



Request to access from CMP Web page or by E-mail to :
cmp@imag.fr

The user receive by E-mail the NDA + ARM linary Addendum.

The user sign and return by post 2 original signed copies

CMP forward to Tezzaron the NDAs.

When Tezzaron is OK, they counter-sign and return one copy to CMP.

CMP return the copy to the user and give the access to the DRM and Design-Platform.



Users having access to the Design Platform

CNRS - INPG - UJF

CPPM, Marseille
 IPHC, Strasbourg
 LAL, Orsay
 LPNHE, Paris
 IRFU, CEA Saclay
 LAPP, Annecy-Le-Vieux *
 ENSTA PARISTECH, Paris *

France

INFN, Roma
 INFN, Pavia
 INFN, Pisa
 University of Bologna *
 University of Perugia

Italy

University of Bonn, Germany

University of Barcelona, Spain
 IMSE-CNM-CSIC, Sevilla, Spain

University of Turku, Finland

Acreo AB, Norrköping, Sweden

Norwegian University, Trondheim, Norway

New Users

Tezzaron Semiconductor, USA

FermiLab, USA

North Carolina State University, USA

MOSIS, USA

CMC Microsystems, Canada

University of Sherbrooke, Canada

+ Other centers supported by MOSIS and CMC
 Not listed here.

More than 18 Users in Europe

Conclusion

- ❑ A very collaborative work has been achieved and still ongoing between the parties CMC, CMP, MOSIS, FermiLab, Tezzaron, HEP Labs, NCSU.

A **Unique and Unprecedented** Design Platform resulted from the collaboration.

(Industrial CAD vendors just starting addressing the features)

- ❑ First MPW run deadline : May 31st, 2011
- ❑ The community is awaiting for new CAD tools dedicated to 3D-IC Integration :
 - + 3D-IC Partitioning : both at the system level and the floor-planning level.
 - + Sign-off tools for 3D-IC Integration : (3D-DRC, 3D-LVS, 3D-Extraction)