FD-SOI Technology
- analog/RF/MS focus

Andreia CATHELIN, PhD HDR | STMicroelectronics
Technology R&D Crolles | Design Platform | Senior Member of the Technical Staff
Tel: +33 476926603 | Mobile: +33 607649918 | andreia.cathelin@st.com

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Typical Transistor in today CMOS System on Chip

Change of Substrate adding the thin Buried oxide

Improving power Efficiency – Bringing high flexibility in SoC integration
While keep very similar manufacturing flow
FD-SEI – The Best Technology Choice

Efficient, Flexible & Simple technology

- Outstanding **power efficiency** at every level
- Highly-efficient **RF & analog integration**
- **Back-biasing** as a flexible and powerful optimization
- Extensive existing **fab infrastructure re-use**

Mature Solution & Strong Ecosystem

- **Ecosystem ready** at all stages
- **Extended IP offer**
- **PDK is available** now
- Strategic **collaboration** between Samsung and ST

FD-SEI gives your SOC competitive advantages
Addressing Digital Markets

**FinFet**
- High end servers
- Laptops & tablet-PC

**Ultimate Digital Integration**

**FD-SOI**
- Consumer Multimedia
- Internet of Things, Wearable
- Automotive

**Available from 28nm node**

**Ultimate Digital Integration + AMS + RF + … Integration**
FD-SOI Benefits for IoT

**Challenges**

- **Ultra Low Power SoC**
  - Ultra low voltage operations with high performance
  - e.g. Cortex A53 running at 400MHz @ 0.6V

- **Integration**
  - Easy and efficient SoC analog integration for better interface to the real world and cost savings
  - ADC/DACs, RF, LDOs, …

- **Power / performance Flexibility**
  - Same SoC used from a very low voltage always-on mode to a performance oriented mode to run Android kind of applications
Example: Ultra Low Power in IoT

SoC Architecture

RF
Analytics
CPU & Memories
Power Management

SoC Power Consumption

34 mW*
Power Supply Loss
RF
Analytics
CPU & Memories
Other

<10 mW*
<5 mW**

Previous Generation (40LP)
FD-SOI 28nm
FD-SOI 28nm ULV

X3 to X6 Power Consumption Improvement with FD-SOI

* Measured on Silicon / Product Simulation
** Projection
FD-SOI Technology for SoC integration

- Digital Logic
- Memories
- Analog / RF & High-speed
28nm FD-SOI makes analog/RF/mmW designer’s life easier

- **Improved Analog Performance**
  - Speed increase in all analog blocks
  - Higher gain for a given current density

- **Improved Noise**
  - Lower gate and parasitic capacitance
  - Lower noise variability

- **Efficient Short Devices**
  - Better matching for short devices and efficient design with \( L > L_{\text{min}} \)

- **Very large \( V_T \) tuning range**
  - Wide range of analog parameters tuning via a new independent “tuning knob” (back-gate)

- **Novel flexible design architectures**
- Higher bandwidth
- Lower power
- Smaller designs
- Improved design margins wrt PVT variations
Advantages in Analog Design

**Efficient Short Devices**

- Efficient use of short devices:
  - High analogue gain @ Low L
  - Low Vt mismatch (Avt ~ 2mV/µm)
- Performance example:
  - A 10µm/100nm device has a DC gain of 100, & a σVt of only 2mV!

**Improved Analog Perf.**

- Higher Gm for a given current density
- Lower gate capacitance
- Higher achievable bandwidth or lower power for a given bandwidth

**Improved Noise**

- Same normalized drain current noise between BULK and FD-SOI
- Lower noise variability for FD-SOI
- Improved noise in FD-SOI

Courtesy, L. Vogt, F. Paillardet, C. Charbuillet, P. Scheer, STMicroelectronics
Advantages in Analog Design-II

- **Flip-well devices:**
  - Large Forward Body Bias (FBB) range
  - Negligible control current

- **Use back-gate as « VT tuning knob »:**
  - Unprecedented ~250mV of tuning range for FDSOI vs.
  - ~ 10’s mV in any bulk

Very large $V_T$ tuning range by FBB

![Graph showing $V_T$ tuning range](image)

FD-SOI (flip-well flavor/LVT devices)

![FD-SOI schematic](image)

Courtesy, A. Cathelin, STMicroelectronics
Advantages in MS Design

Variability

- Tighter process corners and less random mismatch than competing processes
- Benefits:
  - Simpler design process, shorter design cycle
  - Improved yield or improved performance at given yield

Switch performance

- Improved gate control allows smaller VTH
- Backgate bias allows for VTH reduction by tuning
- Results is an unprecedented quality of analog switches
- Key for high performance data converters and other Switched-Cap. Circuits
- Compounding benefits: smaller R -> smaller switch -> compact layout -> lower parasitics -> even smaller switch

Lower capacitance

- Lower junction capacitance makes a substantial difference in high-speed circuits
  - Drastic reduction of self-loading in gain stages
  - Drastic reduction of switch self-loading
- Two-fold benefit:
  - Leads to incremental improvements
  - Allows the designer to use circuit architectures that would be infeasible/inefficient in bulk technologies

Courtesy, S. Le Tual, STMicroelectronics; B. Murmann, Stanford Univ.
RF CMOS device figures of merit

• High Frequency Figures of Merit for RF circuits

\[
f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}
\]

\[
f_{\text{max}} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_s) + 2\pi f_T R_g C_{gd}}}
\]

\[
NF_{\text{min}} = 1 + K \cdot \frac{f}{f_T} \cdot \sqrt{1 + g_m(R_g + R_s)}
\]

Maximizing RF performance:

- **\( f_T \)** is given for a technology node, and scales favorably in nanometer CMOS.
- **\( NF_{\text{min}} \) & \( f_{\text{max}} \)** are negatively impacted by the gate resistance and extrinsic layout access resistances which should be minimized.

- **\( f_T \)**
  
  Relates to current gain, \( \Leftrightarrow \) how fast transistors can charge (loading) capacitors.
  
  \( f_T \) is more relevant for high-speed circuits.

- **\( f_{\text{max}} \)**
  
  Relates to power gain, \( \Leftrightarrow \) maximum gain reachable for an amplifier.
  
  \( f_{\text{max}} \) is more relevant for RF and mmW circuits.
RF CMOS device
28nm UTBB FD-SOI Layout example

- Straight to the top
  - Minimize thin metal and vias access resistance

- Staggered Drain/Source metal straps
  - Tradeoff between fringing capacitance and current density

- Double gate access
  Gate is strapped with metal 1 and 2

- Body Bias ring

Courtesy, L. Vogt, F. Paillardet, C. Charbuillet, P. Scheer, STMicroelectronics
UTBB 28nm FD-SOI RF and mmW Performance

- Benchmark for LVT NMOS (flip-well device)

<table>
<thead>
<tr>
<th>Use-case</th>
<th>28FDSOI Low Power GHz range</th>
<th>28FDSOI (intrinsic model) mmW usage</th>
<th>28FDSOI (extrinsic model) mmW usage</th>
<th>28 LP bulk (intrinsic model) mmW usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wfinger (µm)</td>
<td>1.2</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>L (nm)</td>
<td>100</td>
<td>30</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Idens (µA/µm)</td>
<td>125</td>
<td>200</td>
<td>200</td>
<td>300</td>
</tr>
<tr>
<td>NFmin (dB)</td>
<td>0.5 @ 10GHz</td>
<td>1.3 @ 60GHz</td>
<td>1.4@60GHz</td>
<td>n.a.</td>
</tr>
<tr>
<td>Ft (GHz)</td>
<td>100</td>
<td>335</td>
<td>238</td>
<td>270</td>
</tr>
<tr>
<td>Fmax (GHz)</td>
<td>n.a.</td>
<td>355</td>
<td>324</td>
<td>315</td>
</tr>
<tr>
<td>MAG (dB)</td>
<td>12 @ 10GHz</td>
<td>12 @ 60 GHz</td>
<td>10 @ 60GHz</td>
<td>n.a.</td>
</tr>
<tr>
<td>DC Gain (dB)</td>
<td>40</td>
<td>18</td>
<td>18</td>
<td>17</td>
</tr>
<tr>
<td>σVt (mV)</td>
<td>1.5</td>
<td>2</td>
<td>2</td>
<td>3</td>
</tr>
</tbody>
</table>

Courtesy, L. Vogt, F. Paillardet, C. Charbuillet, P. Scheer, STMicroelectronics
Analog/RF/mmW Design examples in FD-SOI
On the usage of FBB for inverter-based Analog/RF 28nm UTBB FDSOI: example of a 450MHz Gm-C filter with IIP3> 1dBv over a 0.7-1V power supply

[J. Lechevalier at al, ISSCC2015]
Analog/RF design in FD-SOI

• FD-SOI arguments:
  • FBB as VT tuning knob ➔ ultra large tuning range for VT
  • Very good analog performance ➔ lower power consumption and operate at L>Lmin for design margin

• Consequences on analog/RF design:
  • Operate amplifiers at constant Gm
  • Employ new tuning strategies
  • Competitive noise and linearity behavior
  • Obtain strong design independence with respect to PVT variations

• New robust design opportunities
Motivation

• Analog filters are generic blocks for any type of wireless communication systems

• Filters with several 100’s MHz bandwidth
  – Energy efficient wireless communication SoC’s
  – Need to tune independently several parameters impacting overall system:
    • cut-off frequency,
    • linearity,
    • noise,
    • all for an optimal power consumption

• Inverter-based analog functions are attractive implementations (Gm-C filters, variable amplifiers, …)
Inverter based transconductor

• High Dynamic Range per power

• No internal nodes
  – Wideband Gm

• Negative resistance
  – \( Z_{\text{differential}} = \frac{1}{g_{\text{mc}}-g_{\text{mb}}} \)
  – High DC gain

• Common mode control
  – \( Z_{\text{common}} = \frac{1}{g_{\text{mb}}+g_{\text{mc}}} \)
Inverter-based filters

- Tuned by supply voltage

- LDO Regulator
  - Voltage headroom
  - Power
Eliminate the regulator by using FD-SOI technology

- Tuned by supply voltage

- LDO Regulator
  - Voltage headroom
  - Power

- Regulator drop (>20\%)
- Tuning margin
- Filter supply
- Global supply
Non-matched $\beta_n$ & $\beta_p$ \hspace{1cm} ($\beta = \mu C_{ox} \frac{W}{L}$)

- Non-linearity
- Distortion
\[ \beta_n = \beta_p \]
\[ \beta_n < \beta_p \]

The diagram illustrates a differential amplifier circuit with voltage and current relationships.
**Type of operation**

**Ideal (calculated)**
- Square law devices
- Constant gm

**Real devices**
- Mobility reduction
- Triode region
- Exponential region

**OK:** gm variation; **NOK:** linearity, noise variation
Fixed supply operation, tune by Vbody

- Eliminate LDO regulator
- $$V_{\text{Filter}} = V_{\text{DD}}$$
FD-SOI CMOS operation specific

FD-SOI: Tuning gm with Vbody

OK: gm variation; OK: linearity, noise constant

- Compensate $V_{\text{DD}}$ variations
  - tune gm back to nominal
  - constant $f_C$ & linearity
  - Without regulator

![Graphs showing gm variation with and without back-gate bias](image)
Filter Implementation

- LC ladder prototype
  - 3\textsuperscript{rd} order Butterworth low-pass Gm-C filter

- Impedance scaling
  - L > L_{\text{min}} improves r_{\text{out}}
    - L = 110\text{nm} for all transistors
    - Better linearity & matching

- Filter area: 0.04 mm\textsuperscript{2}
  - Gm's: ~0.01 mm\textsuperscript{2}
  - Capacitors: ~0.03 mm\textsuperscript{2}
Cut-off frequency tuning

For a fixed VDD operation (0.9V), get wide range Fc tuning by Vbody (Gm variation by X5)

\[ V_{BBN} = |V_{BBP}| \]
For a wide range of VDD (0.7-1V), get wide range Fc tuning by Vbody
For a desired value of $F_c$, get in-spec linearity $\forall$ $V_{DD}$, by $V_{body}$ tuning.

\[ V_{BBN} = |V_{BBP}| \]
Multiple possibilities, get in-spec linearity ∀ VDD, by independent Vbody tuning
Example of filter performance at Fc=450MHz, at optimum IIP3, tuning by Vbody.

For a wide VDD range, get constant system-level behavior with superb analog features (Fc, linearity, noise).
Comparison with state of the art

Compared to similar circuit implementation in 65nm bulk, at same noise level (impedance level), get X2 linearity for /4 power level

<table>
<thead>
<tr>
<th></th>
<th>This work</th>
<th>[2]</th>
<th>[5]</th>
<th>[6]</th>
<th>[7]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>28nm FD-SOI CMOS</td>
<td>3</td>
<td>3</td>
<td>5</td>
<td>3</td>
</tr>
<tr>
<td><strong>Order</strong></td>
<td></td>
<td>3</td>
<td>3</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td><strong>Supply voltage [V]</strong></td>
<td>0.7 0.8 0.9 1</td>
<td>1</td>
<td>1.2</td>
<td>1.2</td>
<td>1.8</td>
</tr>
<tr>
<td><strong>Cut-off freq. [MHz]</strong></td>
<td>454 454 457 459</td>
<td>4700*</td>
<td>275</td>
<td>200</td>
<td>300</td>
</tr>
<tr>
<td><strong>Input ref. noise</strong></td>
<td>5.9 6.1 6.1 5.9</td>
<td>6.6</td>
<td>7.8</td>
<td>35.4</td>
<td>5</td>
</tr>
<tr>
<td><strong>in-band IIP3 [dBVP]</strong></td>
<td>1.2 4.0 4.0 2.4</td>
<td>-3</td>
<td>-12.5</td>
<td>4</td>
<td>6.9</td>
</tr>
<tr>
<td><strong>Power diss. [mW]</strong></td>
<td>4.0 4.6 5.2 5.6</td>
<td>19c</td>
<td>36</td>
<td>21</td>
<td>72</td>
</tr>
<tr>
<td><strong>SFDR/BW [dB/Hz]</strong></td>
<td>109 110 110 109</td>
<td>105</td>
<td>98</td>
<td>100</td>
<td>113</td>
</tr>
</tbody>
</table>

* excluding LDO regulator + tuning voltage headroom  

* Higher Fc obtained only by capacitor scaling

[^2]: HoufAf, et al., ISSCC 2012  
[^5]: Saari, et al., TCAS-I 2009  
[^6]: Mobarak, et al., JSSC 2010  
[^7]: Kwon, et al., TMTT 2009
Comparison with state of the art

Compared to best-in-class active RC filter, at same noise level (impedance level) and Fc, get decent linearity for /14 power level

<table>
<thead>
<tr>
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<td>3</td>
</tr>
<tr>
<td>Order</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply voltage [V]</td>
<td>0.7</td>
<td>0.8</td>
<td>0.9</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Cut-off freq. [MHz]</td>
<td>454</td>
<td>454</td>
<td>457</td>
<td>459</td>
<td>4700</td>
</tr>
<tr>
<td>Input ref. noise [nVrms/√Hz]</td>
<td>5.9</td>
<td>6.1</td>
<td>6.1</td>
<td>5.9</td>
<td>6.6</td>
</tr>
<tr>
<td>in-band IIP3 [dBVp]</td>
<td>1.2</td>
<td>4.0</td>
<td>4.0</td>
<td>2.4</td>
<td>-3</td>
</tr>
<tr>
<td>Power diss. [mW]</td>
<td>4.0</td>
<td>4.6</td>
<td>5.2</td>
<td>5.6</td>
<td>19</td>
</tr>
<tr>
<td>SFDR/BW [dB/Hz]</td>
<td>109</td>
<td>110</td>
<td>110</td>
<td>109</td>
<td>105</td>
</tr>
</tbody>
</table>

* Active RC topologies have best-in-class linearity among filters; Gm-C were reputed to have worst linearity

Conclusions

• Inverter based analog/RF design in FD-SOI
  – Added degree of freedom: large $V_T$ tuning by $V_{body}$
  – New robust design opportunities

• 450MHz low-pass Gm-C filter
  – Tuned by back-gate instead of supply
  – Supply regulator-free operation
    • Energy efficient
    • Low voltage
  – Competitive linearity

• Best NSNR of recent Gm-C filters
A 60GHz 28nm UTBB FD-SOI Reconfigurable Power Amplifier with 21% PAE, 18.2dBm P1dB and 74mW PDC

[A. Larie et al., ISSCC2015]
RF/mmW design in FD-SOI

• FD-SOI arguments:
  • FBB as VT tuning knob ➔ ultra large tuning range for VT
  • Very good analog performance ➔ lower power consumption
  • Deep submicron technology:
    • Front-end: performant \( f_T, f_{\text{max}} \)
    • Back-end + FD-SOI features: performant passive devices

• Consequences on RF/mmW design:
  • New family of reconfigurable topologies; new design architectures
  • State of the art implementations with concomitant optimisation for each system-level parameter

New robust design opportunities
Motivation

WiGiG (OFDM-based) => max. operation probability @ 8dB back-off ➔ high linearity with optimized power

50% power in mmW TRx spent in PA

Solve the general trade-off linearity and efficiency (PAE)
Schematic

- Segmented-bias (class-AB / class-C) to improve linearity and dc consumption
Segmented-bias (class-AB / class-C) to improve linearity and dc consumption

- Operating class controlled by back-gate voltages $V_{B1}$ and $V_{B2}$
  - No splitter needed as gates can be connected
  - Highly efficient compact alternative to Doherty PA
Reconfigurable linearized power cell - III

- Segmented-bias (class-AB / class-C) to improve linearity and dc consumption

- Operating class controlled by back-gate voltages $V_{B1}$ and $V_{B2}$
  
  $\rightarrow$ No splitter needed as gates can be connected
  
  $\rightarrow$ Highly efficient compact alternative to Doherty PA

- Capacitive neutralization with MOS device to track $C_{gd}$
  
  $\rightarrow$ Better immunity to process and bias variations
PA topology

NRPC : Neutralized Reconfigurable Power Cell
CL : Coupled Lines

Area_{CORE} : 0.16mm²
NRPC : Neutralized Reconfigurable Power Cell
CL : Coupled Lines

10 ML stack
Strict density rules
Less than 1dB IL
Small-signal measured results

PA gain and linearity modes configured by body bias only, fixed VDD

- S-parameters results at VDD=1.0V
- Two highlighted modes: high gain & high linearity (intermediate modes possible)
- > 8 GHz bandwidth
- Unconditionally stable
Large-signal measured linearity results

The power gain and linearity can be continuously tuned thanks to the body bias. When the high linearity mode is reached, the power gain is totally flat which boosts the linearity.

<table>
<thead>
<tr>
<th>mode</th>
<th>Gain [dB]</th>
<th>$P_{1dB}$ [dBm]</th>
<th>PAE$_{1dB}$ [%]</th>
<th>$P_{DC}$ [mW]</th>
<th>PAE$_{8dB_backoff}$ [%]</th>
<th>$P_{diss@8dB_backoff}$ [mW]</th>
<th>$100\times P_{1dB}/P_{DC}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>High gain mode</td>
<td>35</td>
<td>15</td>
<td>9</td>
<td>331</td>
<td>1.5</td>
<td>331</td>
<td>9.6</td>
</tr>
<tr>
<td>High linearity mode</td>
<td><strong>15.4</strong></td>
<td><strong>18.2</strong></td>
<td>21</td>
<td>74</td>
<td><strong>8</strong></td>
<td>124</td>
<td><strong>89</strong></td>
</tr>
</tbody>
</table>

Continuous tuning
### Table: Performance Comparison

<table>
<thead>
<tr>
<th></th>
<th>This work</th>
<th>S. Kulkarni JSSC 2014</th>
<th>D. Zhao JSSC 2013</th>
<th>D. Zhao JSSC 2012</th>
<th>E. Kaymaksut RFIC 2014</th>
<th>A. Siligaris JSSC 2010</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>28nm UTBB FD-SOI</td>
<td>40nm</td>
<td>40nm</td>
<td>40nm</td>
<td>40nm</td>
<td>65nm PD-SOI</td>
</tr>
<tr>
<td><strong>Operating mode</strong></td>
<td>High gain, High linearity</td>
<td>NA</td>
<td>Low/High power</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td><strong>Supply voltage [V]</strong></td>
<td>1.0</td>
<td>1.0</td>
<td>0.8</td>
<td>0.9</td>
<td>1.0</td>
<td>0.9</td>
</tr>
<tr>
<td><strong>Freq. [GHz]</strong></td>
<td>61</td>
<td>60</td>
<td>60</td>
<td>63</td>
<td>61</td>
<td>60</td>
</tr>
<tr>
<td><strong>Gain [dB]</strong></td>
<td>35</td>
<td>15.4</td>
<td>15.1</td>
<td>22.4</td>
<td>16.8 / 17</td>
<td>26</td>
</tr>
<tr>
<td><strong>P_{SAT} [dBm]</strong></td>
<td>18.9</td>
<td>18.8</td>
<td>16.9</td>
<td>16.4</td>
<td>12.1 / 17</td>
<td>15.6</td>
</tr>
<tr>
<td><strong>P_{1dB} [dBm]</strong></td>
<td>15</td>
<td>18.2</td>
<td>16.2</td>
<td>13.9</td>
<td>9.1 / 13.8</td>
<td>15.6</td>
</tr>
<tr>
<td><strong>PAE_{max} [%]</strong></td>
<td>17.7</td>
<td>21</td>
<td>21</td>
<td>23</td>
<td>22.2 / 30.3</td>
<td>25</td>
</tr>
<tr>
<td><strong>PAE_{1dB} [%]</strong></td>
<td>9</td>
<td>21</td>
<td>21</td>
<td>18.9</td>
<td>14.1 / 21.6</td>
<td>25</td>
</tr>
<tr>
<td><strong>PAE_{8dB_backoff} [%]</strong></td>
<td>1.5</td>
<td>8</td>
<td>7.5</td>
<td>3</td>
<td>- / 4.7</td>
<td>5.8</td>
</tr>
<tr>
<td><strong>P_{DC} [mW]</strong></td>
<td>331</td>
<td>74</td>
<td>58</td>
<td>88</td>
<td>56 / 75&quot;</td>
<td>117</td>
</tr>
<tr>
<td><strong>P_{DC_{8dB_backoff}} [mW]</strong></td>
<td>332</td>
<td>124</td>
<td>84</td>
<td>94</td>
<td>56 / 78&quot;</td>
<td>120</td>
</tr>
<tr>
<td><strong>100xP_{1dB}/P_{DC}</strong></td>
<td>9.6</td>
<td>89</td>
<td>72</td>
<td>28</td>
<td>14.5 / 32&quot;</td>
<td>31</td>
</tr>
<tr>
<td><strong>Active area [mm²]</strong></td>
<td>0.162</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ITRS FOM [W.GHz²]</strong></td>
<td>161,671</td>
<td>1,988</td>
<td>1,198</td>
<td>6,925</td>
<td>641 / 2,832</td>
<td>13,009</td>
</tr>
</tbody>
</table>

ITRS FOM = \( P_{SAT} \cdot PAE_{\text{max}} \cdot \text{Gain}\cdot \text{Freq}^2 \)

* with pads

# : estimated

**Comparison with state of the art**

Performant gain, \( P_{\text{SAT}} \), linearity and efficiency thanks to FD-SOI technology and low-loss power combiner. Improves ITRS FOM by x10.
The high linearity mode reduces the dissipated energy at 8dB back-off with no compromise in linearity.

<table>
<thead>
<tr>
<th>Technology</th>
<th>This work</th>
<th>S. Kulkarni JSSC 2014</th>
<th>D. Zhao JSSC 2013</th>
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<td>Operating mode</td>
<td>High gain</td>
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<td>NA</td>
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<tr>
<td>Supply voltage [V]</td>
<td>1.0</td>
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<tr>
<td>Freq. [GHz]</td>
<td>61</td>
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</tr>
<tr>
<td>Gain [dB]</td>
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<td>P_{SAT} [dBm]</td>
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<td>13.9</td>
<td>9.1 / 13.8</td>
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<tr>
<td>PAE_{max} [%]</td>
<td>17.7</td>
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<td>22.2 / 30.3</td>
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<td>1.5</td>
<td>8</td>
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<td>3</td>
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<td>ITRS FOM [W.GHz²]</td>
<td>161,671</td>
<td>1,988</td>
<td>1,198</td>
<td>6,925</td>
<td>641 / 2,832</td>
<td>13,009</td>
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ITRS FOM = P_{SAT}.PAE_{max}.Gain.Freq²  
*: with pads  #: estimated
Comparison with state of the art

FD-SOI enables low supply low power operation still with high performance results.

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\text{ITRS FOM} = P_{\text{SAT}} \cdot \text{PAE}_{\text{max}} \cdot \text{Gain} \cdot \text{Freq}^2
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\(^{*}\): with pads
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Comparison with state of the art – system-level performance

**Previous references**
- Zhao, *JSSC* 2013
- Siligaris, *JSSC* 2010
- Kulkarni, *ISSCC* 2014
- Kaymaksut, *RFIC* 2014

**This work**
(high linearity mode)

*Best linearity/consumption tradeoff!*
• Fully WiGiG compliant (linearity and frequency range)

• Reconfigurable power cells:
  • Continuous tuning thanks to body bias with 2 extreme modes:
    • High gain mode: Highest ITRS FOM
    • High linearity mode: Break the linearity/consumption tradeoff
  • High efficiency @ large output power back-off
  • Optimization of the transmitter line-up depending on modulation and output power
Conclusion
FD-SOI Takeaways for Analog/RF/mixed-signal

• FD-SOI arguments:
  • For Analog/RF design:
    • FBB as VT tuning knob ➔ ultra large tuning range for VT
    • Very good analog performance ➔ lower power consumption and operate at L>Lmin for design margin
  • For RF/mmW design, operate at Lmin and add:
    • Deep submicron technology features:
      • Front-end: performant $f_T$, $f_{max}$
      • Back-end + FD-SOI features: performant passive devices
  • For mixed-signal/high-speed design:
    • Improved variability
    • Switch performance
    • Reduced parasitic capacitance