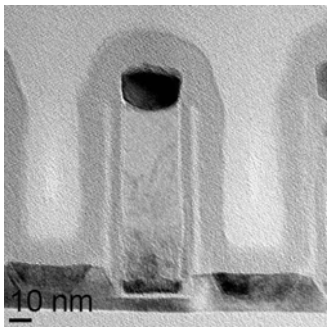
CEA-LETI R&D 20nm Fully Depleted SOI Multi-Project Wafers

For years, LETI has pioneered the development of Fully-depleted Silicon on Insulator (FDSOI) technology, demonstrating the advantages of this technology over bulk conventional technology for future nodes. In particular, excellent electrostatic integrity of the transistors is ensured by the thinness of the body, without the need of extra litho steps or channel doping. This leads to a planar device technology that exhibits excellent short channel behavior and record variability results, as shown in a number of recent papers. With this Multi-Project Wafers (MPW) initiative, LETI offers through CMP to the R&D design community the opportunity to implement innovative designs on this technology.



- Specific acceptance rules
  - No commercial products
  - No military or medical application circuits
- Main technology features
  - High-k / metal gate stack
  - Transistor gate lengths down to 25nm
  - 4 levels of metallization with 65nm ground rules
  - Single threshold voltage n- and p-MOSFETs with balanced Vth of ±0.4V
- PDK content and associated documentation
  - FDSOI compact model with typical and corners model cards (Compact Model User Manual),
  - Parameterized cells and pads for the physical implementation
  - Physical verification files for DRC/LVS (Design Rules Manual),
  - Characterized Digital Standard cells library (40 cells)
  - PDK Reference Manual
  - Design Rules Manual